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Voltage Mode First Order All Pass Filter Design Using DX-MOCCII

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Abstract: in this paper a voltage mode first order all-pass filter is designed using dual X multi output second generation current conveyor (DX-MOCCII). This all pass filter is designed using one DX-MOCCII, one resistor and one capacitor. Non-ideal analysis and parasitic effect on DX-MOCCII based filter is also presented here. PSPICE simulation results agree well with the proposed theory.

Keywords: All-pass filter, DX-MOCCII, Voltage mode, Analog Building Block.

I. INTRODUCTION

In many analog signals processing application all-pass filter is a very simple and useful analog building block. In recent years an analog building block have great attention for designing circuits due to their low power consumption, wide band width, high slew rate, great linearity etc. It is used in instrumentation system, in communication, in delay equalization etc. Over a wide frequency range it provides 90^0 delays to the applied input signal.

In the literature there are various voltage mode analog building block based all-pass filter such as second generation current conveyor (CCII) [1.2], differential difference current conveyor (DDCC) [3] four terminal floating nullator (FTFN) [4], current differencing buffered amplifier(CDBA) [5], differential voltage current conveyor (DVCC) [6], dual output current conveyor (DOCCII) [7], dual X current conveyor(DXCCII) [8] etc.

In this paper a new voltage mode all-pass filter is designed using one analog building block, two passive components. The circuit is based on DX-MOCCII. The proposed circuit is simulated through Cadence ORCAD PSPICE simulator using 0.25µm TSMC CMOS process parameter.

II. DX-MOCCII BUILDING BLOCK

The block diagram, CMOS circuit diagram of DX-MOCCII is shown in Fig.1 and Fig.2 respectively. In this block diagram X_p is the non-inverting and X_n is the inverting terminal is conveying signal to the Z_p and the Z_n terminal.

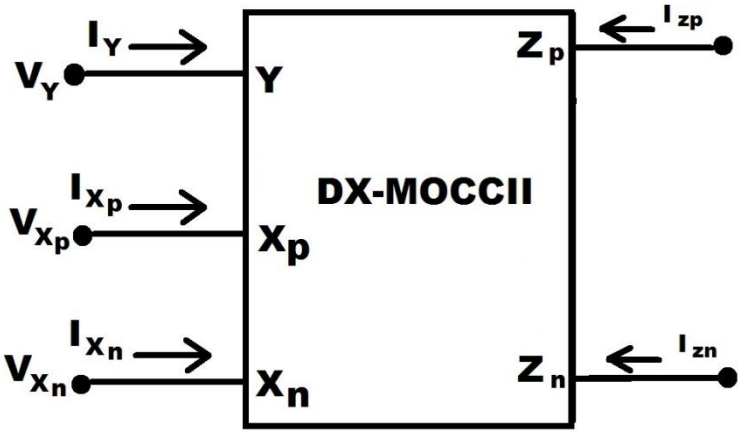

Fig.1: Block diagram of DX-MOCCII

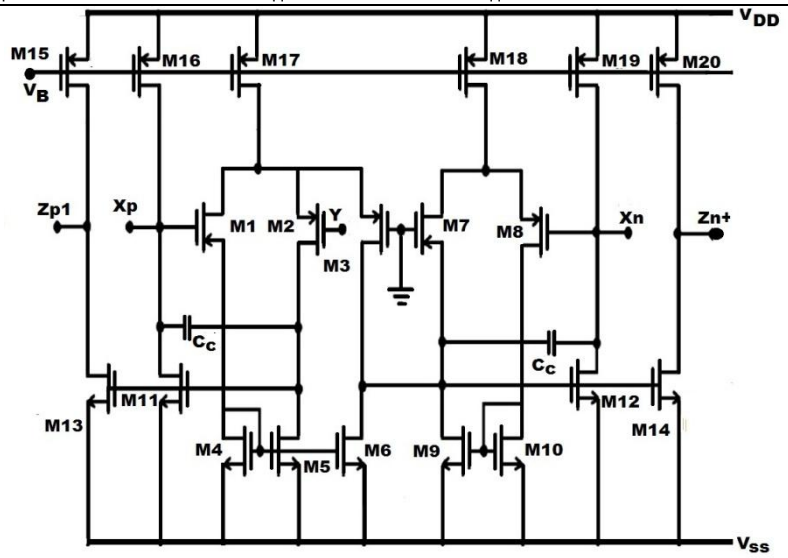

Fig.2: CMOS circuit diagram of DX-MOCCII

DX-MOCCII is characterized by the following port relationship

$$\begin{bmatrix} I_y \\ V_{xp} \\ V_{xn} \\ I_{zp_i} \\ I_{Zn_j} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_{xp} \\ I_{xn} \end{bmatrix} \quad (1)$$

Where i=1,2,…..,4 and j=1,2,….,6. Ideally in DX-MOCCII, y terminal has high impedance so no current flows in y terminal, x_p is the non inverting and x_n is the inverting port, z_p, z_n port has high output impedance of the DX-MOCCII building block.

III. PROPOSED ALL PASS FILTER CIRCUIT

The voltage mode all-pass filter circuit using DX-MOCCII is shown in Fig.3. Routine analysis of the circuit gives the following transfer function.

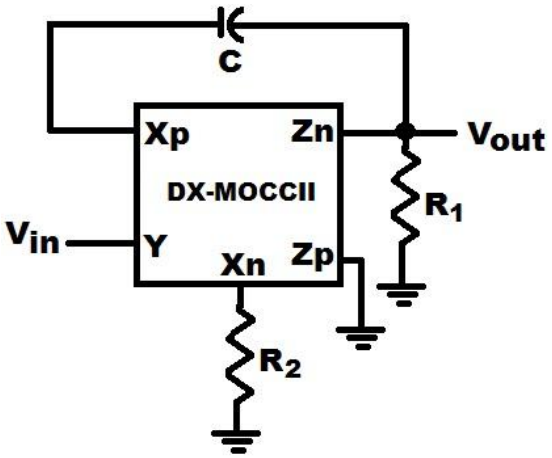

Fig.3: Proposed All-pass filter

$$\frac{V_{out}}{V_{in}} = \frac{sCR_2 - 1}{sCR_1 + 1} \quad (2)$$

Phase response of the proposed circuit is given by

$$\varphi(\omega)=180^0-2\tan^{-1}(\omega RC) \quad (3)$$

Here pole frequency is given by

$$\omega_0=\frac{1}{RC} \quad (4)$$

Sensitivity of the proposed all-pass filter circuit w.r.t various components can be expressed as:

$$S_{R_1R_2}^{\omega_0}=-1, S_C^{\omega_0}=0 \quad (5)$$

Sensitivity of the pole frequency ω_o are small and its maximum value is -1

IV. NON-IDEAL ANALYSIS OF THE PROPOSED CIRCUIT

Non-ideality due to transfer gain:

The matrix equation due to non ideal characteristics can be expressed as:

$$\begin{bmatrix} I_y \\ V_{xp} \\ V_{xn} \\ I_{zp_i} \\ I_{zn_j} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_p & 0 & 0 \\ -\beta_n & 0 & 0 \\ 0 & \alpha_{p_i} & 0 \\ 0 & 0 & \alpha_{n_j} \end{bmatrix} \begin{bmatrix} V_y \\ I_{xp} \\ I_{xn} \end{bmatrix} \quad (6)$$

Here β_p,β_n are voltage transfer gain of X_p and X_n port respectively. A_p, α_n are current gain from X_p and X_n port to Z_p and Z_n port respectively.

The modified equation for series inductor can be written as:

$$\frac{V_{out}}{V_{in}}=\frac{\beta_p sCR_2-\alpha_n}{sCR_1+1} \quad (7)$$

Non-ideality due to parasitic components:

The parasitic model of DX-CCII is shown in Fig.4. Here R_y, R_{zp}, R_{zn} have high parasitic resistance value and is attached with Y, Z_p, Z_n port respectively. R_{xp}, R_{xn} are low parasitic resistance connected in series with X_p , X_n terminals. C_{xp}, C_{xn} parasitic capacitance has very low value connected in X_p, X_n terminals.

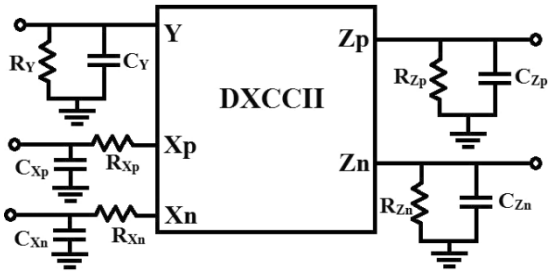

Fig.4: Parasitic model of DX-CCII

Transfer function obtained using the above approximation is

$$\frac{V_{out}}{V_{in}}=\left(\frac{C}{C+C_{Zn}}\right)\left(\frac{s-1/CR_{equ}}{s+1/R'(C+C_{Zn})}\right) \quad (8)$$

Where, $R_{equ}=R_1+R_{xn}$ and $R'=R//R_{zn}$

V. SIMULATION RESULTS

The proposed all-pass filter in Fig.3 is simulated by PSPICE simulator using 0.25µm TSMC level-3 technology parameter. Supply voltage taken as $V_{DD} = V_{SS} = \pm 1.25V$, and $V_B = -0.3V$. The length and width ratio of various MOSFET transistor of DX-MOCCII is given in Table-1. Proposed all pass filter is designed using C=45pF, and R_1=1.5KΩ, R_2=3KΩ with a pole frequency 2.36MHz. The gain and phase response of all pass filter is shown in Fig.5. Transient response of all pass filter is also shown in Fig.6. Frequency spectrum of the

input and output signal is shown in Fig.7. 90^0 phase shift between the input and output signal is shown in Fig.8 which confirms the quadrature relationship between input output waveform.

Table-1: Aspect ratio of various transistors

Transistors	**Aspect ratio W(µm)/L(µm)**
M_1,M_2,M_4,M_5, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}	2/.25
M_3, M_6, M_7, M_8, M_9, M_{10}	4/.25
M_{11}, M_{12}, M_{13}, M_{14},	16/.25

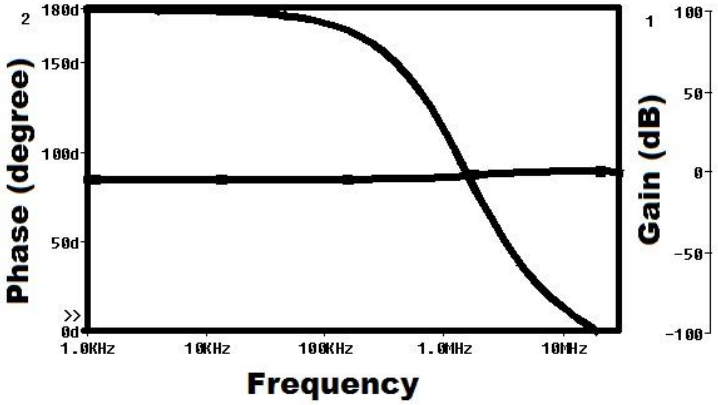

Fig.5: Gain and Phase response of proposed circuit

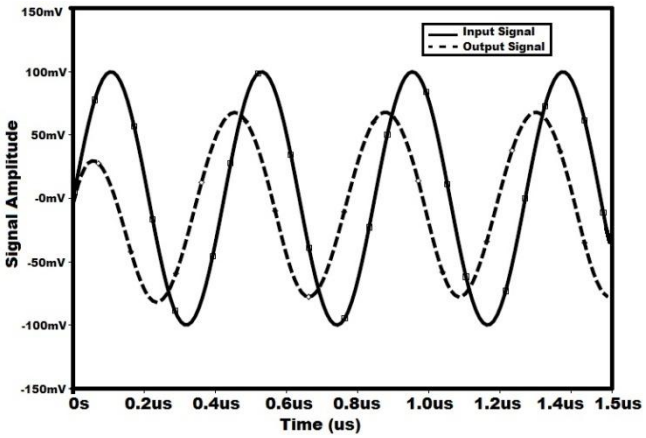

Fig.6: Time domain response of proposed all pass filter

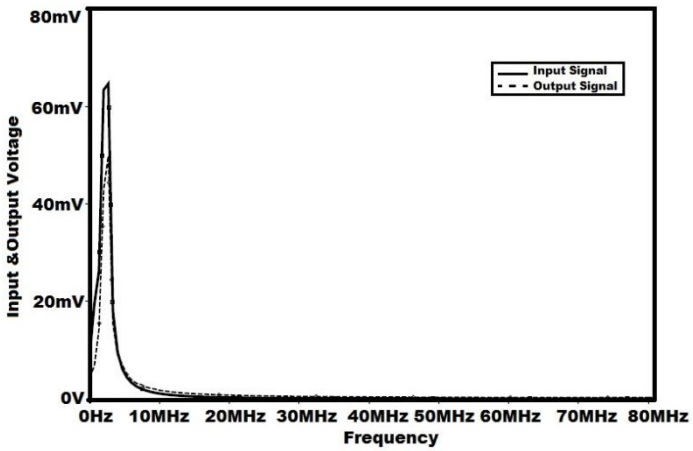

Fig.7: Frequency spectrum of input, output signal

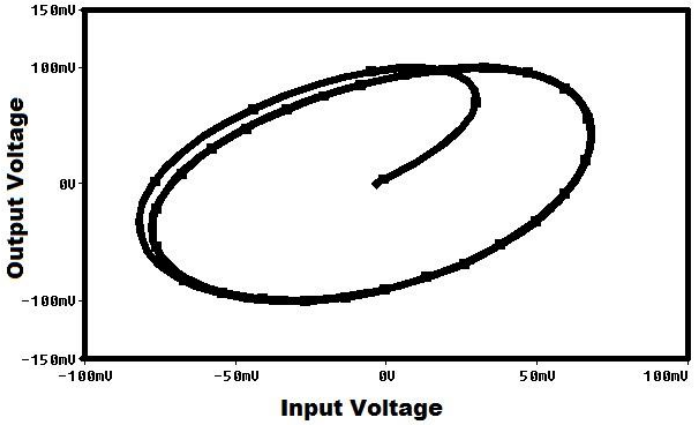

Fig.8: Lissajous figure of APF

VI. CONCLUSION

Here a voltage mode all pass filter is designed using a single DX-MOCCII building block, one capacitor and two resistors. Sensitivity with respect to various passive components are found to be very small and unity in magnitude. Simulated results agree well with the proposed theory.

REFERENCES

[1] N. Pandey, and S.K. Paul, "All-pass filters based on CCII– and CCCII–", International Journal of Electronics, vol. 91, no. 8, pp. 485 - 489, 2004.

[2] B. Metin, A. Toker, H. Terzioglu, and O. Cicekoglu, "A new all-pass section for high-performance signal processing with a single CCII-", Frequenz, vol. 57, no. 11, pp. 241-243, 2003.

[3] M.A. Ibrahim, S. Minaei, and E. Yuce, "All-pass sections with high gain opportunity", Radioengineering, vol. 20, no. 1, pp. 3-9, 2011.

[4] M. Higashimura, "Current-mode allpass filter using FTFN with grounded capacitor," *Electronics Letters*, vol. 27, no. 13, pp. 1182– 1183, 1991.

[5] A. Toker, S. ¨ Ozoguz, O. C¸ ic¸ekoglu, and C. Acar, "Current-mode all-pass filters using current differencing buffered amplifier and a new high-Q bandpass filter configuration," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 9, pp. 949–954, 2000.

[6] S. Minaei and M. A. Ibrahim, "General configuration for realizing current-mode first-order all-pass filter using DVCC," *International Journal of Electronics*, vol. 92, no. 6, pp. 347–356, 2005.

[7] S. Minaei and E. Yuce, "All grounded passive elements currentmode all-pass filter," *Journal of Circuits, Systems and Computers*, vol. 18, no. 1, pp. 31–43, 2009.

[8] S. Minaei and E. Yuce, "Unity/variable-gain voltage-mode/current- mode first-order all-pass filters using single dual-X second-generation current conveyor," *IETE Journal of Research*, vol. 56, no. 6, pp. 305–312, 2010.