International Journal of Latest Engineering and Management Research (IJLEMR)
ISSN: 2455-4847
www.ijlemr.com || Volume 02 - Issue 04 || April 2017 || PP. 50-55

A CMOS dynamic logic circuit using FCR

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Abstract: Due to the superior speed and area characteristics, dynamic circuits are widely applied in data paths and other time critical components in modern microprocessors. The high switching activity of dynamic circuits, however, consumes significant power. In this project, a p-type/n-type dynamic circuit selection (PNS) algorithm and a flexible charge recycling (FCR) design methodology are proposed to achieve high power efficiency in data paths. The effects of technology scaling, data path width, design complexity, clock skew and environmental conditions are discussed. Simulation results shows that the power consumption of an arithmetic and logic unit (ALU) with the proposed PNS-FCRcan be reduced by up to 60% as compared with a conventional ALU.

I. Introduction

Over the past four decades, the number of transistors in a chip has grown continuously. With an increasing transistor density, the power consumption of
microprocessors has become a major design issue for a wide range of applications, from ultralow power medical sensors to high performance microprocessors in leading servers. As a fundamental part of modern microprocessors, data paths perform computing operations, typically along the critical path. The operating speed of the data paths usually determines the achievable operating frequency of the entire microprocessor. At the same time, the data path is one of the most active components and consumes a significant share of the total power consumption. This situation is further exacerbated for those applications with an intensive computation, such as digital signal microprocessors and multimedia processors with multiple cores. Hence, it is vital to achieve low power data paths in modern
microprocessors.

Due to the superior speed and area characteristics, dynamic circuits are widely applied in data paths and other time critical paths. For example, in the 32-nm Intel Itanium microprocessor, code named Poulson, and the 32-nm AMD microprocessor, code named Bulldozer, the on-chip memory and arithmetic and logic unit (ALU) adopt n-type dynamic circuits to minimize latency. However, since the dynamic circuits are usually cascaded to form domino CMOS logic, each stage of dynamic logic requires a static CMOS inverter to ensure that all inputs to each stage are maintained low during the precharge phase. This property makes synthesizing dynamic circuits with Computer Aided Design (CAD) tools more difficult than synthesizing static CMOS circuits. In addition, the varying characteristics of different types of dynamic circuits (n-type and p-type) increase the design complexity of a data path. Unfortunately, the existing solutions are not sufficient to solve these issues. In this paper, a novel p-type/n-type dynamic circuit
selection (PNS) algorithm and a flexible charge recycling (FCR) design methodology are proposed, referred to here as PNS-FCR, which targets low power data paths in modern microprocessors.
The primary contributions of this paper are as follows.
1)A novel PNS algorithm is presented to provide charge recycling and explore power saving opportunities for specific applications.
2) A design flow to achieve power efficient data paths is presented.
3) An analysis of power efficiency of the PNS-FCR is provided and an analytical model is described for estimating the power savings of PNS-FCR.
4) A comprehensive suite of simulations is discussed, evaluating the effects of technology scaling, data path width, design complexity, clock skew, and environmental conditions. These simulations demonstrate that PNS-FCR provides low design complexity, good design flexibility, and significant power savings, while achieving the targeted performance objectives of different applications.
5) An ALU IC is described based on a 0.35-μm Global Foundries technology, demonstrating the power and area efficiency of PNS-FCR.

II. Previous Techniques

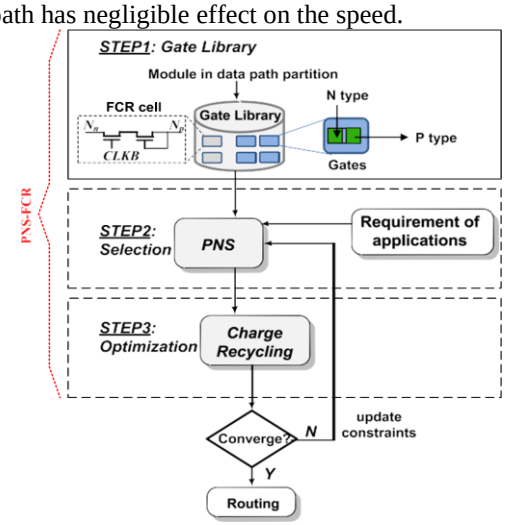
A. PNS-FCR Dynamic circuit Tehnique

The PNS-FCR design methodology comprises of Gate library, PNS (Pmos Nmos Selection) and charge recycling block.

Gate library is made of regular modules of a data path i.e., arithmetic unit, logic unit and bit shift unit. It comprises AND, OR, XOR, shift gate, inverter, carry cell and sum cell of full adder. The operation condition and input-output switching influences the delay and power.

As the gate library selects the peculiar gate to implement the data path in ALU. Multidimensional multiple-choice knapsack problem introduced the PNS algorithm to satisfy the performance . To meet the performance of the data path gates of critical path are essential. To raise the power efficiency, the gates in non-critical path utilizes a low power version.

Two cascaded gates are selected in a critical path one is n-type dynamic gate and other is p-type. During precharge stage through the transistor Pcn Nn node is precharged to Vdd. Whereas the node Np is discharged to ground by the transistor Ncp. Nn is discharged to ground and Np is charged to Vdd during the evaluation phase providing suitable input. The Nn's high state and Np's low state is maintained until the next precharge stage if suitable is not provided in evaluation stage. By the completion of evaluation phase, Nn discharges from high to low and Np is charged from low to high. Nn and Np consumes the dynamic power during precharge phase. By placing the charge recycling circuit in between the pull up and pull down circuits, Nn is charged through Np which reduces the power. Now consider an example shown in the Fig.1 full adder circuit using zipper domino logic. Here Nn is charged by the Np rather than charging through the Pcn. The capacitance cr in the recycling path has negligible effect on the speed.



PNS-FCR FLOWCHART

A. Gate Library

Since the regular modules of a data path (including the arithmetic unit, logic unit, and bit shift unit) are typically designed with basic gates, a gate library is the initial step of PNS-FCR. Based on two types of dynamic circuits, the basic gate library is designed to produce a data path.

The gate library includes AND gate, OR gate, XOR gate, shift gate, inverter, Carry cell and Sum cell of a full adder, and other basic gates. Note that to conveniently exchange gates and modules, two types of each gate occupy similar layout area.

In the gate library, the delay (*D)* and power (*P)* of gates are influenced by the operation condition and the specific input/output switching. Therefore, at the corner of the Process, Voltage, and Temperature (PVT) variations, in the worst case of the input, and with a fan-out of 4, the delay (*D)* and power (*P)* of gates in the gate library are simulated to get the reliable performance. For example, the delay (*D)* and power (*P)* of a two-input OR gate are designed with a fan-out of 4, and are simulated using the SPICE models including PVT variations. At the same time, when one input is transmitted from 1 to 0 or from 0 to 1, the other one keeps 0, the delay is $D1{-}0$ and $D0{-}1$, respectively, then the delay (*D)* is $\text{Max}\{D1{-}0, D0{-}1\}$; when two inputs are simultaneously transmitted from 1 to 0 or from 0 to 1, the power is $P1{-}0$ and $P0{-}1$, respectively, then the power (*D)* is $\text{Max}\{P1{-}0, P0{-}1\}$. What is more, the delay and power of the gates strongly depend on the threshold voltage (*V*th*)* and supply voltage (*V*dd*)*. For a specific *V*th and *V*dd, the power and delay of each gate are characterized.

B. PN Selection Algorithm

Based on the gate library, the appropriate type of gate is selected to implement a data path .To satisfy the performance requirements of different applications, a PNS algorithm is introduced based on the multidimensional multiple-choice 0-1 Knapsack problem (MMKP). The delay of the critical path determines the performance of the data path. The gates in the
critical path are required to meet the performance constraint, while the gates in the noncritical paths use a low power version to enhance power efficiency. The proposed PNS algorithm behaves as follows. Assume n gates are in the critical path. In the gate library, each gate

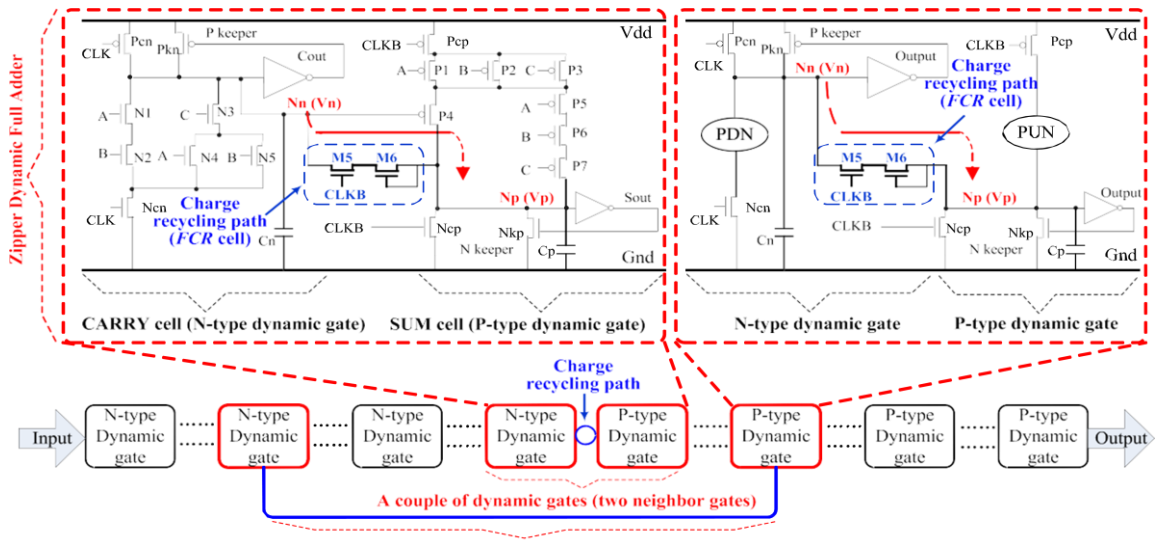
$$\min \text{Max} \sum_{i=1}^{n} \sum_{j=1}^{2} Pi\,j\,(Vth, Vdd)\,xi\,j$$

$$\text{s.t.} \sum_{i=1}^{n} \sum_{j=1}^{2} Di\,j\,(Vth, Vdd)\,xi\,j \le Dc,$$

$$xi\,j \in \{0, 1\},\ i \in [1, n],\ j \in [1, 2]$$

C. Flexible Charge Recycling Technique

A key design issue in low power data paths is exploring the choice of different power efficient n-type and p-type gates. Accordingly, the FCR is proposed to achieve high power Efficiency. Consider a critical data path with two cascaded gates. The initial gate is an n-type dynamic gate, while the latter gate is a p-type dynamic gate. During the precharge stage (CLK = 0), the dynamic node of the n-type gate Nn is precharged to Vdd through transistor Pcn, while the dynamic node of the p-type gate Np is discharged to ground through transistor Ncp. In the evaluation stage, provided that the necessary input combination is applied, Nn is discharged to ground and Np is charged to Vdd. Otherwise, the high state of Nn and low state of Np are maintained until the next precharge stage. As the evaluation process completes, Nn discharges from high to low and Np charges from low to high. In the following precharge stage, Nn and Np both consume dynamic power by charging Nn from Vdd and discharging Np to ground. If a switch is inserted between the two dynamic gates, Nn is charged by Np through a charge recycling path, thereby reducing the dynamic power. Toward this direction, a zipper dynamic full
adder is taken as an example. When the input vectors of full adder are respectively (1, 1, 0), (1, 0, 1), and (0, 1, 1), at the end of an evaluation stage, Nn has been
discharged to Gnd while Np has been charged to Vdd, and the switch is turned on. And then, a desirable charge recycling path between Nn and Np is built. The voltage waveforms of
Nn and Np, when full adders are without and with FCR cell, are shown in Fig. 4. With the FCR cell, in the precharge stage, the CLKB makes the recycle path available.



PROPOSED FCR TECHIQUE

D. Power Efficiency of PNS-FCR

An analytic model is provided for the power reduction factor αi . A couple of dynamic gates (one n-type dynamic gate and one p-type dynamic gate) are taken as an example. During a clock cycle (including the evaluation and precharge phases), the total energy Et , dissipated by
one n-type dynamic gate and one p-type dynamic gate. Once a charge recycling path is determined, at the end of the evaluation phase, Cp is charged to Vdd and Cn is discharged to ground. The precharge phase arrives and the charge recycling process is enabled. Cn is charged by Cp until the voltage of Np(Vp) and Nn (Vn) reaches Vp = Vn + Vth,

E. Design Flow for a Data Path Based on FNS-FCR

The design flow for a data path based on FNS-FCR is as following:

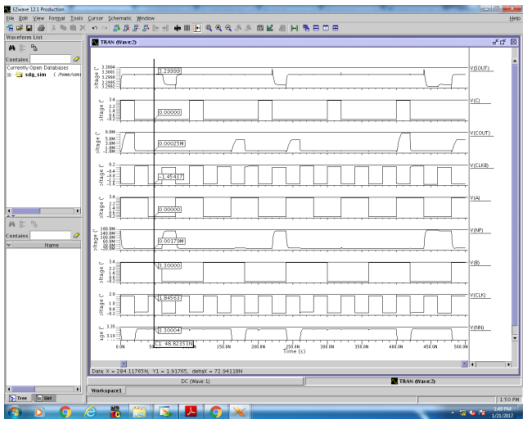
1) First, the gate library based on a p-type/n-type dynamic circuit is built. Two types of each gate occupy similar layout area to avoid the area penalty.
2) Based on the gate library, the appropriate type of gates is selected using PNS to implement the data path or critical path, satisfying the performance requirements of different applications.
3) Next, the FCR is utilized to achieve high power efficiency in critical path by inserting the charge recycling paths between two independent gates or two neighboring gates. Note that the FCR is a tradeoff between power, performance, and silicon
area.
4) Then, apply the proposed PNS-FCR to noncritical paths. The critical path is typically much longer than uncritical path in the data path, and therefore, the gates in the uncritical path employ p-type for power efficiency. However, if an uncritical path formed by all p-type gates is even slower than the critical path, n-type gates would be inserted to meet the delay constraint based
on PNS, and then the FCR is used to enhance the power efficiency.
5) Finally, the routing is completed manually or by CAD tools.

III. Experimental Results

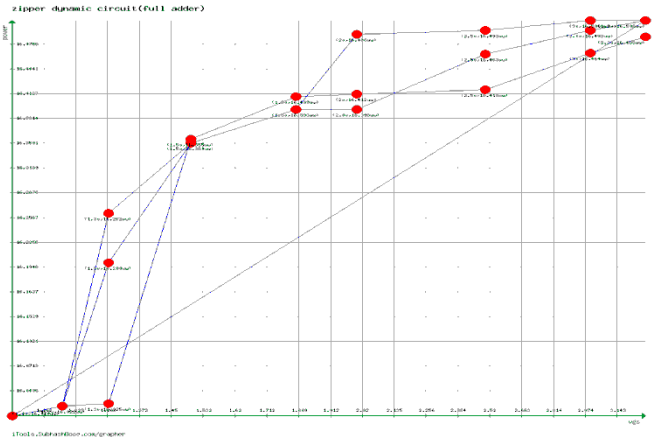
Verification of FCR:

To verify the effectiveness of FCR, a full adder with clock-delay as designed, which is usually employed along the critical path in data path. A full adder with FCR includes one n-type Sum cell, one p-type Carry cell (dynamic full adder), and one FCR cell to enhance power efficiency. The schematic design of the adder circuit without and with FCR respectively. The output waveforms shows the voltage and dynamic node variation with respect to clk signal.

The adder circuit is designed and it is a dynamic full adder which consumes less power than the conventional adder. This adder circuit has 3 inputs and 2 outputs and the adder is called as ripple carry order where the carry out of one adder is given to the next adder and the carry out is obtained at the last adder circuit. This adder is implemented in ALU in order to achieve high efficiency.



Full adder waveform

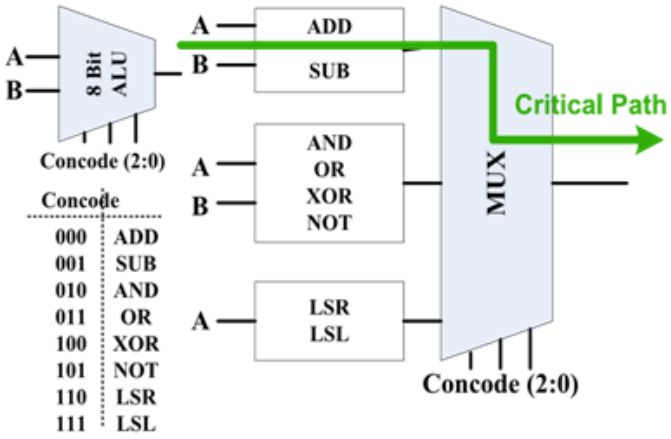


Full adder graph

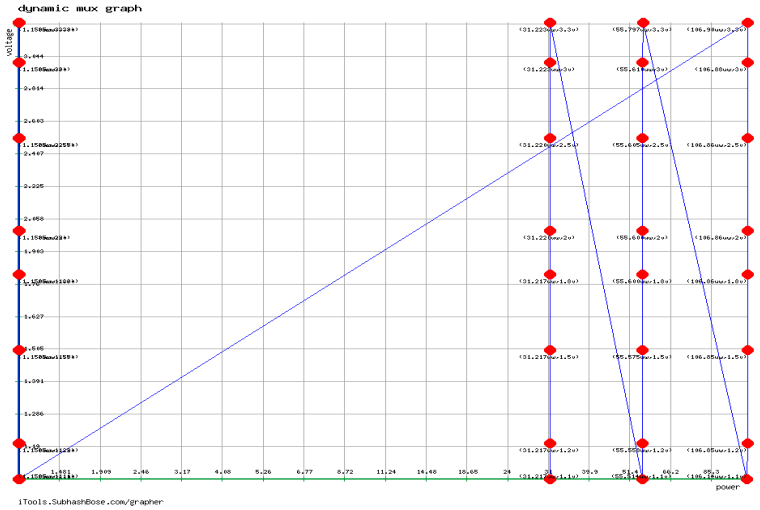
IV. Application To ALU

ALU is partitioned in to functional blocks and control blocks. Functional blocks perform Boolean operations with operands. Boolean operations are AND, OR, XOR, NOR, XNOR. The control unit gives ALU the information that what operation has to be done on that data. The data between the registers, the ALU and

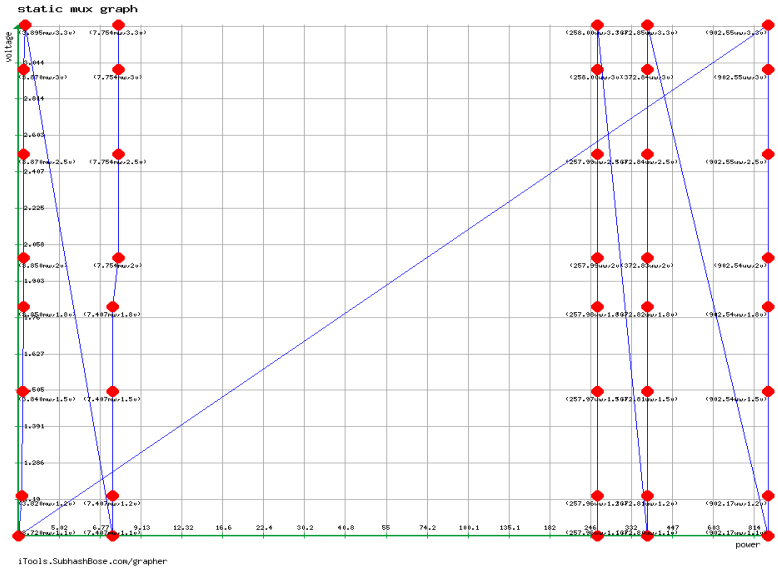
memory can be moved by control unit. The most important components in a microprocessor is ALU and it is the part of the processor. By implementing the ALU, the rest of microprocessor is implemented to feed operands and control codes.



8 BIT ALU



DYNAMIC ANALYSIS GRAPH



STATIC ANALYSIS GRAPH

V. Conclusion

In PNS-FCR methodology achieves high power efficiency, while satisfying specific timing constraints. 8bit-ALU can be reduced by 41% to 60% operating at different frequencies as compared with a conventional ALU.. This methodology can be extended to static CMOS, pass gate, transmission gate, tristate gate, and other logic families.

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