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Optimum Design of Low-Voltage Distributed Photovoltaic Systems Oriented to Enhanced Fault ride Through Capability

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ABSTRACT: The prescribed perspective of high accession of distributed generation photovoltaic (DG-PV) units on low-voltage distribution networks has brought up many issues regarding their performance in case of network transient phenomena. In this study, the design principles that DG-PV units must incorporate in order to meet the requirements of low-voltage ride through capability (LVRTC) are investigated through detailed theoretical analysis and calculations. The analysis shows that a realistic over-sizing of interfaced inverters of DG-PV as well as an appropriate selection of the equivalent interconnecting reactance X_{DG}, in conjunction with high penetration levels, can lead to satisfaction of LVRTC demands without violating the protection limits of the network. Moreover, the scenario of uniform dispersion along the distribution lines is proved rather favorable concerning the demand of LVRTC for voltage selectivity. Finally, considering the derived outcomes, a methodology of optimum design about LVRTC is proposed within the framework of reasonable constraints, which can be applied to any low-voltage distribution network.

KEYWORDS: DG-PV, LVRTC, Reactance, Interfaced Inverters

I. INTRODUCTION

Photovoltaic (PV) power plants are nowadays exhibiting a notable development globally because of substantial advantages, such as flexible installation and minimum upkeep [1, 2]. The aforementioned advantages presage higher levels of PV generation into the energy equilibrium. This is also the aim of various legislation initiatives both in European countries and the United States [3, 4]. The most promising category of PV systems is the grid connected distributed generation PV (DG-PV), as it has been proven very efficient and cost effective [5, 6].

Nevertheless, DG-PV penetration level (PL) today is usually restricted (by distribution companies) to 20% of the substation installed power [7]. In this way, PV production impact on the distribution grid operation, especially in the event of electrical power system unbalance, is significantly reduced. However, such strict constraints hamper the further development and incorporation of renewable energy sources (RESs) into the electrical power systems. To get over this, all RES generators (wind parks, PV systems and so on) have to acquire operating features akin to that of conventional power plants (based on synchronous generators), in order to contribute to a fault event too. Therefore the standard of low-voltage ride through capability (LVRTC) has been adopted in all types of RES attached to high- and medium-voltage grid. In particular, the high power level of wind farms favoured the integration of LVRTC concept in this type of RES and much improvement has already been achieved [8–10]. However, the recent growth of PV plants has led the research community to the implementation of the LVRTC scheme in large-scale PV units (connected to transmission networks) [11, 12].

Regarding the LVRTC scheme, the global energy markets vary. Fig. 1 depicts a typical LVRTC scheme generated by research in many countries such as Germany, Taiwan, North America, Australia, Denmark and so on [13–16]. This scheme describes the desired behaviour of the interconnected units in case of a voltage drop at their point of common coupling (PCC). The time interval that a DG unit has to stay connected to the grid depends on the voltage dip level. Particularly, as the voltage becomes lower, this time interval decreases.

The term of LVRTC is commonly referred to the medium voltage network because of the power level of interconnected units and their weight for the system's proper operation. Considering the low-voltage distribution network, the applied practice until recently enforces the DG units to trip almost immediately under faulty conditions, in order to ensure the smooth operation of the rest of the network. However, the above rigorous policy does not seem to be in force anymore, and voltage support techniques injecting reactive power to the grid have been suggested [17, 18]. Furthermore, the expansion perspective of RES and especially of DG-PV units in distribution networks requires an alternative response of them, in order to achieve high PL.

In particular, the case of low-voltage distributed PV generator (LVDG-PV) systems is of great importance since these small-scale systems (usually lower than 10 kW) can be easily installed in the urban environment, as building incorporated with minimum technical works [19, 20]. In this direction, there is a considerable activity in LVDG-PV installations on buildings' surfaces today, as well as small PV parks [21, 22].

Taking into account the above-mentioned aspects, in this paper, the standard of LVRTC is extended so as to include the DG-PV units that are connected to the low-voltage network. The adoption of LVRTC at the low-voltage network has been recently applied in [23, 24], so this research field seems to be very promising for both researchers and manufacturers. Hence, the interfaced inverters are obliged to be coupled with the low-voltage network and feed the faulty part for time intervals that last more than a few line cycles. Therefore they have to be dimensioned for a significantly longer duration of faulty conditions, calling for more effective thermal management and much higher overcurrent and overvoltage strength. This over-dimensioning (OD) of PV inverters has already been proposed in the technical literature [25, 26] so as to maximise the annual energy harvest. In this paper, the necessary inverter over-sizing is thoroughly investigated in order to meet LVRTC requirements.

The effects of LVRTC application on LVDG-PV systems are discussed in this paper, focusing especially on the case of high PL. Studies about the PL limits of PV units have been recently presented [27, 28], but they only examine the impact of PL on steady-state analysis, that is, for load flow studies. In this paper, the inverter design is taken into account and the investigation of PL parameter is extended in terms of meeting the current LVRTC requirements. Moreover, the necessary adjustments that these units have to incorporate are emphasised in order to fulfil these new operational demands, improving so distribution network during disturbances. General LVDG-PV design guidelines are presented in Section 2, through a detailed theoretical analysis. Finally, an optimum design is proposed in Section 3 regarding the selection of X_{DG} and the higher possible PL achievement, in order to come up effectively against the emerging problems of LVRTC application at the low-voltage network.

II. HEADINGS

2. LVDG-PV design guidelines according to LVRTC
3. Optimum design of LVDG-PV systems

III. INDENTATIONS AND EQUATIONS

1. LVDG-PV design guidelines according to LVRTC

The primary idea of the LVRTC scheme, according to Fig. 1 is to avoid the unnecessary concurrent breakdown of multiple generation sources during a network disturbance. In more details, generation sources have to stay connected to the low-voltage network for time duration which is a function of their 'electrical distance' from the faulty network part. The electrical distance is expressed by the voltage dip at DG's PCC, and hence the term of voltage selectivity is defined. Thus, in cases of short duration faults, generation loss is limited to the ones being close to the faulty network part. This characteristic is crucial for the high expansion of DG-PVs in the direction of high PL realisation.

Note that in high-voltage transmission systems, a fault affects mainly the units that are electrically close to the disturbance. On the contrary, distribution networks usually have a radial structure. Therefore, according to the LVRT scheme, the DGs have to feed the faulty part, since there is no alternative distribution path. Therefore the interfaced inverters owe to be designed in order to create the required voltage selectivity, feeding so the fault with higher currents than the nominal ones for the required interval imposed by the LVRT standard. This trend has been already followed by some inverter manufacturing companies, and so today there are available commercial inverters that are supporting such high overcurrent during short-term disturbances and so on LVRTC [29, 30].

The above features infer that the DG units have to obtain the performance of the synchronous generator during a disturbance. By adjusting the operational behaviour of conventional synchronous generators to LVRTC terms, the DG units have to withstand short-circuit currents higher than their nominal values, since they shall be disconnected after at least 0.15 s (according to Fig. 1), reaching so steady-state faulty conditions. Hence, it is preferable for the LVDG-PV units to behave as voltage sources during disturbances instead of acting as constant current sources (providing slightly higher than their nominal AC current value during disturbances). Nevertheless, the LVDG-PV units can be suitably controlled in order to decrease the significant deviation between transient and steady-state currents [31, 32].

The suggested design concept has some important aspects that should be investigated thoroughly. First of all, the LVDG-PV units have to behave as a voltage source in series with a reactance. This means that voltage source inverters are more likely to incorporate this operational behaviour. Moreover, the inverter control algorithm needs to be redefined. In contrast to the current fast response during disturbances, the critical

issue in case of a high PL value is a suitable response – so as to meet the desired voltage drop selectivity (defined by the LVRTC scheme). Similar approaches have been presented at various inverter topologies in [23, 33]. Particularly, the inverter control signal retains its pre-disturbance value in order to avoid unnecessary generation divergences in case of short-term disturbances. Hence, the equivalent voltage source of the LVDG-PV unit remains close to its steady-state value (similar to conventional generators). However, if the disturbance duration is longer, the inverter controller is triggered either to reduce the current within safe limits or trip the LVDG-PV unit if the time limit (defined by LVRTC scheme) is exceeded.

Next, a design guide will be presented based on the general low- voltage network form (considering one distribution line for simplicity reasons), taking into account that all connected LVDG-PV units act as conventional AC voltage sources under faulty conditions (according to the above analysis).

A three-phase low-voltage network with DG-PVs, operating under unity power factor in steady state is considered. If a three-phase short circuit occurs at the *i*-bus, then the single-phase equivalent circuit of Fig. 2 stands. A similar modelling of distribution network equipped with DG units for disturbance studies has already been presented in [34]. The three-phase short circuit is used for dimensioning the network's protection equipment, so the worst case is included.

The calculation of bus voltages after a fault is carried out through the superposition process, which is absolutely equivalent to the classic method (Y_{bus}) [35]. However, it offers a better sense of the radial distribution network passive elements, which affect the bus voltages after a three-phase short circuit.
Considering a three-phase short circuit at the *i*-bus in Fig. 2, the voltage at *k*-bus is derived from the sum of contributions from all sources. Particularly, for $k<i$ it can be calculated as follows

$$\boldsymbol{V}_{k,\text{SC}i}\big|_{k<i} = \boldsymbol{V}_{k\to k,\text{SC}i} + \boldsymbol{V}_{lv\to k,\text{SC}i} + \sum_{j=1}^{k-1} \boldsymbol{V}_{j\to k,\text{SC}i} + \sum_{j=k+1}^{i-1} \boldsymbol{V}_{j\to k,\text{SC}i} \qquad (1)$$

Similarly, for the buses that are on the right side of the short-circuited bus (k > i), the following expression stands

$$\boldsymbol{V}_{k,\text{SC}i}\big|_{k>i} = \boldsymbol{V}_{k\to k,\text{SC}i} + \boldsymbol{V}_{lv\to k,\text{SC}i} + \sum_{j=i+1}^{k-1} \boldsymbol{V}_{j\to k,\text{SC}i} + \sum_{j=k+1}^{n} \boldsymbol{V}_{j\to k,\text{SC}i} \qquad (2)$$

The calculation of the individual terms in (1) and (2) arises from the superposition principle of sources. The analytical equation set is exhibited in Table 1.
The mathematical expressions for $Z_{k,\text{L}}$, SC*i* and $Z_{k,R,\text{SC}i}$ are given in Appendix.

It is worth mentioning that if there is no generation or load at *k*-bus, the above equations stand if $E_{\text{DG}k}$ becomes zero and $X_{\text{DG}k}$ and Z_{Lk} become infinite, for the specific *k*-bus. Considering that the DG PVs supply only active power in steady state, the internal voltage of a DG connected to the *k*-bus is modelled as follows

$$P_{\text{DG}k} = \frac{\left|\boldsymbol{E}_{\text{DG}k}\right| * V_k * \sin\delta_k}{X_{\text{DG}k}} \qquad (12)$$

Furthermore, as the DGs operate under unity power factor, the following equations stand

$$P_{\text{DG}k} = V_k * I_{\text{DG}k} \qquad (13)$$

$$\tan\delta_k = \frac{X_{\text{DG}k} * I_{\text{DG}k}}{V_k} \qquad (14)$$

Combining (14) and (15) the following expressions can be given

$$\tan \delta_k = \frac{X_{\mathrm{DG}k} * P_{\mathrm{DG}k}}{V_k^2} \qquad (15)$$

Finally, from (12) to (15) the $E_{\mathrm{DG}k}$ can be extracted as

$$\boldsymbol{E}_{\mathrm{DG}k} = \frac{P_{\mathrm{DG}k} * X_{\mathrm{DG}k}}{V_k * \sin\left(\tan^{-1}\left(\frac{X_{\mathrm{DG}k} * P_{\mathrm{DG}k}}{V_k^2}\right)\right)} \angle \tan^{-1}\left(\frac{X_{\mathrm{DG}k} * P_{\mathrm{DG}k}}{V_k^2}\right) \qquad (16)$$

Equation (16) shows that the internal voltage of DG units depends on steady-state parameters at their PCC, that is, the bus voltage and the DG active power. The pre-fault bus voltages and the *LV* voltage are extracted from the load flow analysis. It is obvious that if P_{DG} varies, these voltages change. It has to be mentioned once again that the previous analytical equations (1)–(16) apply only at typical distribution networks with radial structure.

Finally, taking into account (1)–(16), the DG contribution to a fault current in case of a DG connected to the *k*-bus is given by

$$\boldsymbol{I}_{\mathrm{DG}k,\,\mathrm{SC}i} = \frac{\boldsymbol{E}_{\mathrm{DG}k} - \boldsymbol{V}_{k,\,\mathrm{sc}i}}{\mathrm{j}X_{\mathrm{DG}k}} \qquad (17)$$

The above calculation set (1)–(17) can be used as a simplified tool for the estimation of the necessary series inductance as well as of the equivalent AC voltage source for each LVDG-PV unit, so as to achieve the desired voltage drop selectivity. It is obvious that generation units that are on the left side of the short-circuit location are in a more convenient situation, because the voltage at these buses has an additional component because of the upstream network ($Vl_{V\rightarrow k,\mathrm{SC}i}$).

A typical example on how the above equation set can be used for the achievement of the necessary voltage drop selectivity is the determination of the minimum bus voltage. Minimum voltage conditions occur at *n*-bus if the short circuit takes place at its neighbouring bus. Therefore the worst case is a short circuit at $n-1$ bus, because it leads *n*-bus to its smallest possible voltage level (excluding the case of short circuit at *n*-bus itself). For the aboveworst case, equation set (1)–(11) describes the root-mean-square (rms) voltage at the terminal bus as follows (assuming that $|Z_{\mathrm{L}n}| \gg |Z_{\mathrm{LV}n}|$)

$$\boldsymbol{V}_{n,\,\mathrm{SC}n-1} = \boldsymbol{V}_{n\rightarrow n,\,\mathrm{SC}n-1} = \boldsymbol{E}_{\mathrm{DG}n}\frac{1}{1+(\mathrm{j}X_{\mathrm{DG}n}/\boldsymbol{Z}_{\mathrm{LV}n})} \qquad (18)$$

Considering that the internal rms-voltage of LVDG-PV unit is roughly1 pu (in order to generate power under unity or slightly leading power factor), we come up with the marginal minimum rms-voltage at a 'healthy' bus

$$V_{\min,\,\mathrm{rms}}(\mathrm{pu}) = \frac{1}{d_{\min}}, \quad d_{\min} = \left|1 + \frac{\mathrm{j}X_{\mathrm{DG}n}}{\boldsymbol{Z}_{\mathrm{LV}n}}\right| \qquad (19)$$

Fig.3 depicts $V_{\mathrm{min,rms}}$ as a function of $d_{\min}$ in the context of a design example, considering a specific LVRTC scheme (also presented in the same figure). As it can be observed, by setting $d_{\min}$ value, a minimum voltage level can be achieved in case of a three-phase short circuit at the neighbouring bus. More specifically, according to the example of Fig. 3, the selection of $d_{\min}$ below 6.5 reassures that voltage at 'healthy' buses

(even at the neighbouring ones) shall always be >0.15 pu and so they have to stay connected for at least 0,625 ms (more than 30 line cycles in 50 Hz systems). In this way, the philosophy of LVRTC is served and so impermanent faulty conditions would have limited impact on the available DG-PV power production. Of course, the exact definition of $d_{\min}$ has to take into account the corresponding LVDG-PV unit short-circuit level.

The previous analysis can be generalised by considering additional distribution lines with dispersed generation. These lines would be connected in parallel to the bus '0' of Fig. 2 and (1) and(2) would be adjusted. A typical distribution network of the Greek Public Power Corporation S.A. was evaluated in a previous published work [36]. The network under study is summarised in Fig. 4.

Specifically, the authors' study in [36] was conducted in order to ascertain the aspects of DG affecting the bus voltages after a fault occurrence. According to the results of this paper, the bus voltages may become higher by selecting smaller X_{DG} values, but at the same time the DG contribution to fault currents are also increasing even in an in admissible degree for the common design limits of DG power converters. Thus, a compromise about the selection of X_{DG} value is necessary in order to meet the LVRTC demands without contravening the design limits (especially the maximum short-circuit current) of the grid-tied inverter. Finally, an additional important outcome was that the full dispersion of DGs along the distribution lines is deemed rather advantageous regarding the LVRTC demands

2. Optimum design of LVDG-PV systems

The scope of DGs' design optimisation process is the suitable selection of XDG and PL values in the direction of buses voltages' upkeep in the highest possible levels (under faulty conditions). This requirement restricts the impact of the potential impermanent disturbances on the DG-PV power production. It has to be noted that the proposed optimisation process is conducted at a given network with equal DG-PV units (similar to that in Fig. 4), but it can be easily applied at any distribution network with increased DG-PV penetration. The first step in optimisation problems is the definition of an objective function with one or more variables.

Through the maximisation or minimisation (depending on the case) of the objective function, the optimum values for these variables are extracted.

Concerning the typical distribution network presented in Fig. 4, the objective function consists of the sum of buses' voltages after a fault in line 1. Moreover, the transformer installed power is 400 kVA and the grid loading is set to 68% with a typical power factor equal to 0.85. The parameters of the optimisation function are the X_{DG} reactance and the PL value. In this paper, the definition of PL is based on the total load demand and is given by the following equation

$$\mathrm{PL}(\%) = \frac{\sum P_{\mathrm{DG}}}{\sum s_{\mathrm{LOAD}}} \times 100\% \qquad (20)$$

Today, the commercial inverters are able to supply an overcurrent up to 2.8 times the I_{DG} for several milliseconds during disturbance intervals [29, 30]. Moreover, considering that this policy has been recently applied for power quality improvement on autonomous LV–PV systems [37, 38], the factor OD_k at k-bus is defined as follows

$$\mathrm{OD}_k(\%) = \left(\frac{d_k * I_{\mathrm{DG}k}}{I_{\mathrm{DG}k-\mathrm{tr}}} - 1 \right) \times 100\% \qquad (21)$$

The above factor denotes the percentage of DG-PV inverter necessary OD in order to meet the LVRTC requirements.

The objective function and the optimisation constraints are summarised in Table 2.

The scope of the objective function is its maximisation, that is, the maximisation of bus voltages in order to satisfy the LVRTC demands respecting the DG-PV units' OD constraint $\mathrm{OD}_{\mathrm{limit}}$ and the network short-circuit current protection limits I_{SC}. The optimisation process has been conducted for different $\mathrm{OD}_{\mathrm{limit}}$ values. It is noted that the actual PV inverter design and control, according to the current standards [13–15], does not allow contribution to fault currents higher than 120% of the nominal value. However, many recent published papers controvert this rigorous policy, regarding the DG current [25, 26, 29]. Hence, in the current paper, various $\mathrm{OD}_{\mathrm{limits}}$ are studied in order to realise how this factor affects the voltage selectivity achievement under high PL values. It has to be clarified that the PL value varies between 20 and 120%; such PL values do not cause voltage rise issues and so the bus voltages under steady-state conditions are at acceptable levels, according to the EN50160 standard [39].

Fig. 5 presents the optimum X_{DG} value as a function of PL, for different $\mathrm{OD}_{\mathrm{limits}}$; it is clear that the higher $\mathrm{OD}_{\mathrm{limit}}$ makes possible the achievement of voltage selectivity under a wider range of PL values. For

example, if OD_{limit} is set equal to 100%, high-voltage selectivity may be achieved under any PL value between the prescribed ranges.

Additionally, Fig. 6 presents the percentage of buses with voltage higher than 0.1 pu as a function of PL, with OD_{limit} being a parameter, in case of a short circuit at 1LV1 bus. It has to be noted that Fig. 6 refers to a short circuit at 1LV1 bus, which is the worst case regarding the voltage levels. The results in Fig. 6 agree with the ones in Fig. 5, highlighting the fact that more buses may preserve adequately high-voltage levels as OD_{limit} increases. Assuming that this disturbance is temporary, the selection of OD_{limit} and the respective optimum X_{DG} value can be set so as to preserve a critical amount of DG-PVs in operation, especially for high PL values. Obviously, under smaller PL values (e.g. 30 or 40%) the DG-PV generation is less critical and so there is no point trying to preserve considerable generation capacity under the worst faulty conditions. Finally, an important outcome of this optimisation process is that the aforementioned results, regarding the X_{DG} optimum value, do not remarkably violate the protective limits of the distribution network. This is shown in Fig. 7, where the ratio of 1LV5 bus short-circuit current is presented as a function of the PL value, with OD_{limit} being a parameter. Particularly, the I_{SC} varies between 1 and 1.35. Mostly, for a moderate and realistic choice of OD_{limit} lower than 20%, the I_{SC} value comes below 1.2 pu. Therefore the proposed design of DG-PV units can be implemented with minimum reconfigurations in the network protection scheme. Meanwhile, it can be deduced that the restriction of $I_{SC} < 1.2$ pu still permits the achievement of voltage selectivity under a wide PL range, as long as OD_{limit} is higher than 25%.

A complete example of the optimum design of inverter for a given set of specifications is subsequently presented, clearly emphasising the optimisation part. In particular, consider that a reform of a low-voltage distribution network similar to that of Fig. 4 is planned, including the participation of DG-PVs. The first design issue concerns the maximum PL of PVs that this network can incorporate so as to comply with the network's stability margins. Of course, this decision is taken by the network's operator. If the maximum PL, for example, is defined at 60% and considering uniform PV dispersion along the distribution lines – as this scenario is proved rather favourable according the LVRTC demands for voltage selectivity – the methodology of PV inverter's optimum design can be conducted. The first step of inverter's manufacturer is the choice of inverter's OD. Assuming that the cost must be limited to moderate levels, a choice of OD_{limit} equal to 25% seems to be reasonable. Hence, looking at Fig. 5, the optimum X_{DG} value for LVRTC purposes would be ~0.9 pu. In this case, if a short circuit occurs at the secondary winding of the distribution transformer (worst case), the percentage of buses with voltage higher than 0.1 pu would be 40%, according to Fig. 6. Therefore considering that the disturbance is temporary, the inverter's optimum design can hold a crucial amount of DG-PV in operation. Furthermore, in Fig. 7 the I_{SC} for the aforementioned values of PL and X_{DG} closely reaches the value of 1.1 pu. Hence, the protective limits of the network are not violated (given that the protection scheme must be altered slightly).

Summarising the above optimisation results, it has been established that the achievement of PL levels, in the low-voltage distribution level, considerably higher than the current ones is a realistic target, taking for granted that DG-PV units will be designed and controlled in a way that they can operate similar to conventional synchronous generators. The main design alteration that this concept raises is the OD for any individual DG-PV unit, in order to comply with the current LVRTC scheme. Nevertheless, the optimisation algorithm, which has been proposed in the current paper, manages to keep the inverter over-sizing within rational limits, especially in case of higher PL values, while minimising the effects on the network protection settings. However, it is obvious that the realisation of a PL over 30–40% presumes an adequate established energy storage capacity in order to overcome the stochastic behaviour of RES generation.

IV. FIGURES & TABLES

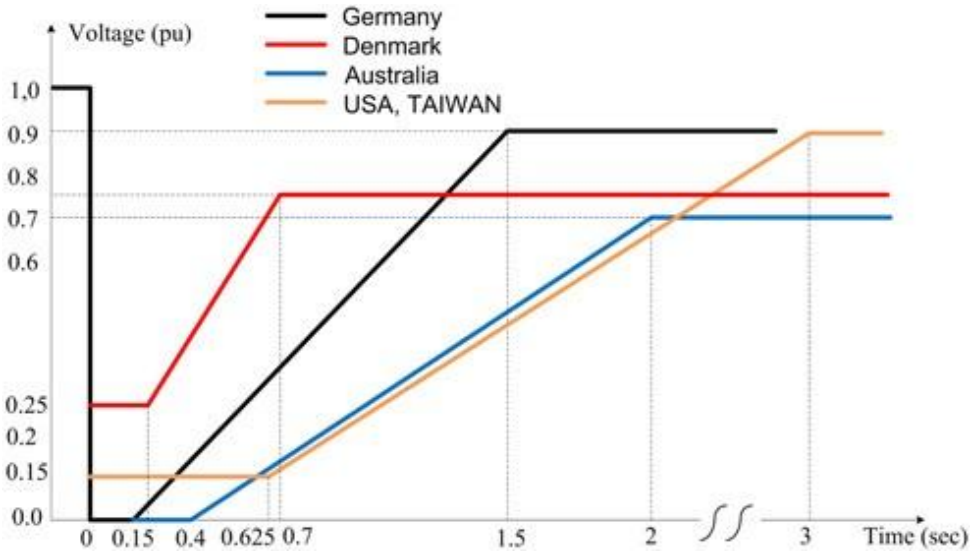

Fig. 1 LVRTC schemes of several energy markets

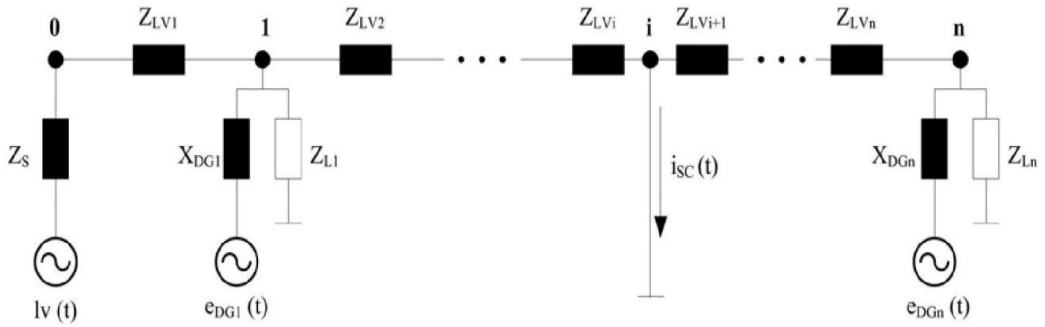

Fig. 2 Single-phase equivalent circuit of LV distribution network line with DG-PV units

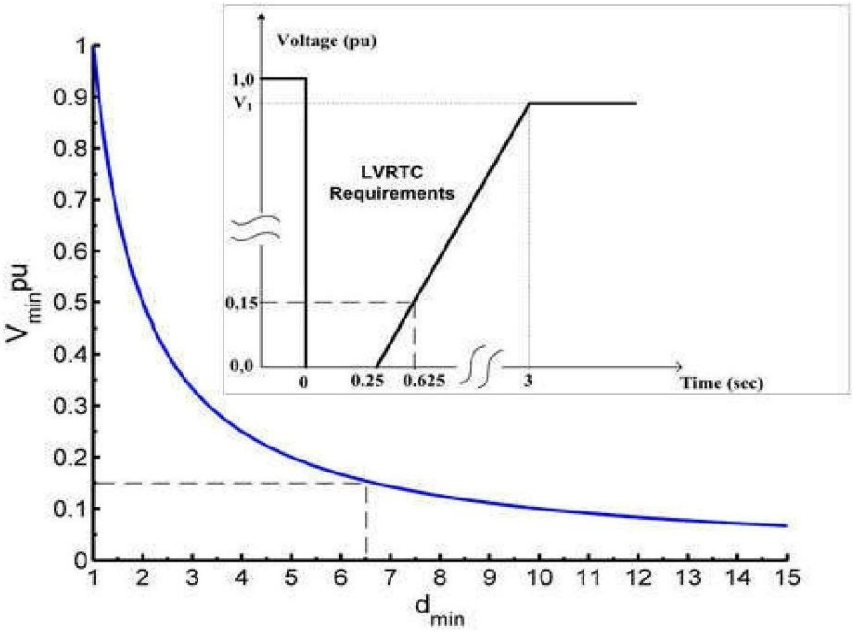

Fig. 3 Example of the proposed LVDG-PV design concept for high PL values

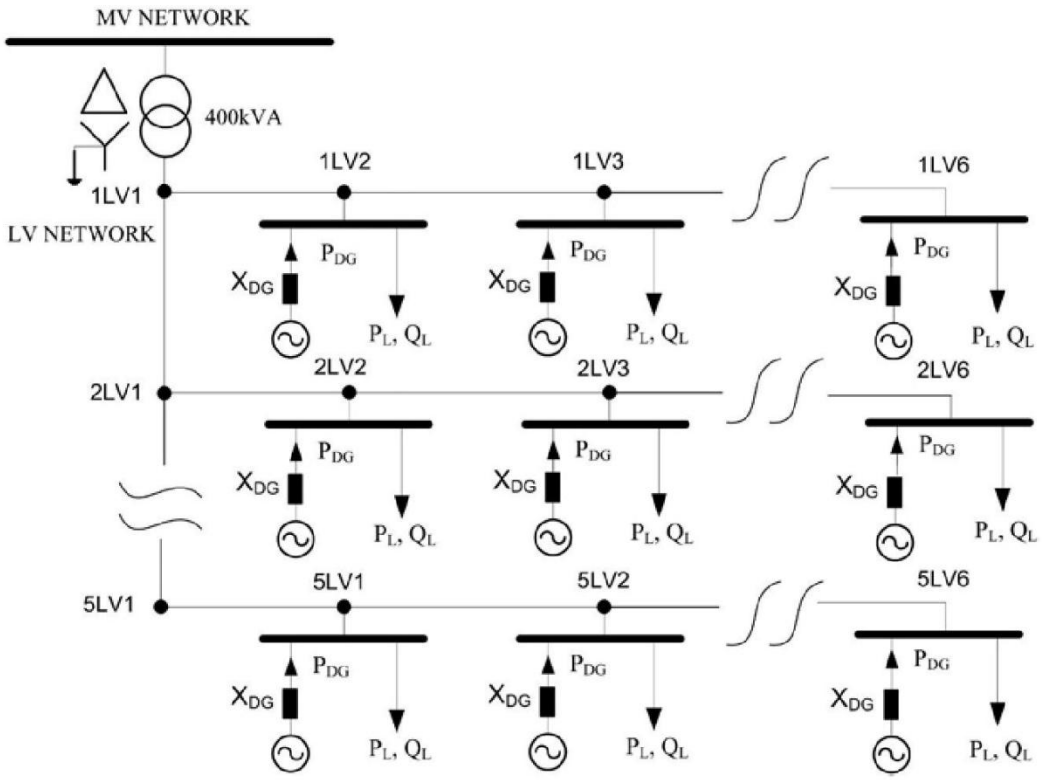

Fig. 4 Layout of distribution network with DG-PV units

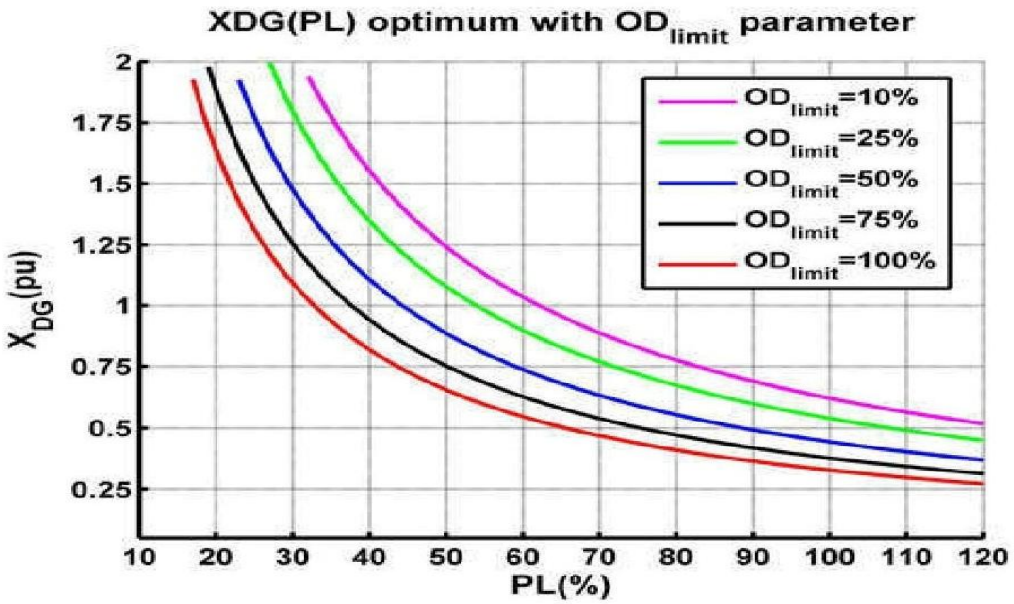

Fig. 5 X_{DG} optimum value as a function of PL for different OD_{limits}

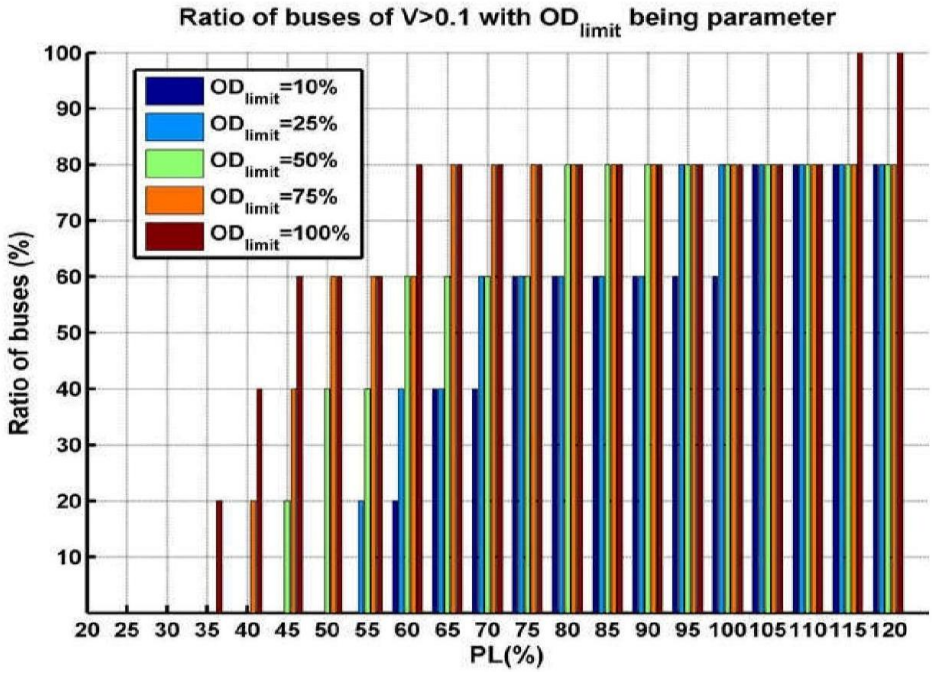

Fig. 6 Percentage of buses with voltage higher than 0.1 pu as a function of PL, with OD_{limit} being a parameter, in case of a short circuit at 1LV1 bus

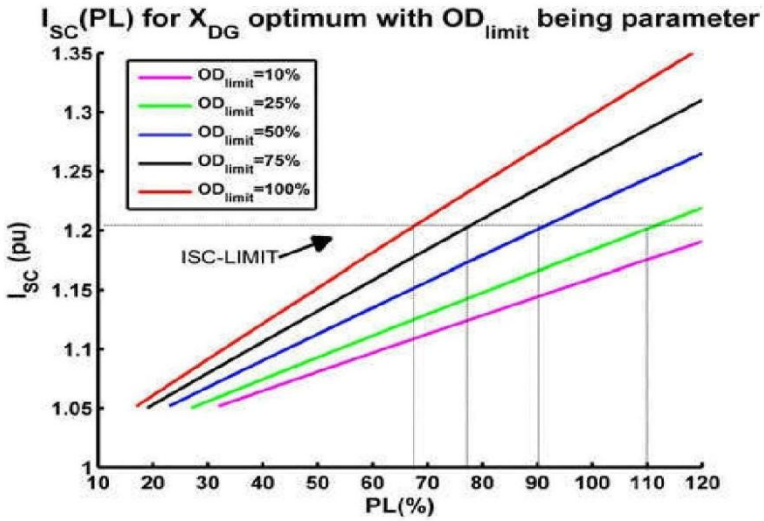

Fig. 7 Impact of optimum X_{DG} and PL values on the ratio of bus short-circuit currents in line 1, in case of a three-phase short circuit at 1LV5 bus (worst case)

Table I Equation set for the analytical calculation of bus voltages after the short circuit

For K<i	*For K>i*
$$V_{k\to k,SCi}\big\vert_{k<i} = E_{DGk}\frac{1}{1+(jX_{DGk}/Z_{k,SCi})} \quad (3$$	$$V_{k\to k,SCi}\big\vert_{k>i} = E_{DGk}\frac{1}{1+(jX_{DGk}/Z_{k,SCi})} \quad (7$$
$$V_{lv\to k,SCi}\big\vert_{k<i} = LV\frac{1}{1+\frac{Z_S}{Z_{0,SCi}}}\prod_{j=0}^{k-1}\frac{Z_{j,R,SCi}-Z_{LVj+1}}{Z_{j,R,SCi}} \quad (4$$	$$V_{lv\to k,SCi}\big\vert_{k>i} = 0 \quad (8$$
$$V_{j\to k,SCi}\big\vert_{j<k<i} = E_{DGj}\frac{1}{1+(jX_{DGj}/Z_{j,SCi})}\prod_{p=1}^{k-1}\frac{Z_{p,R,SCi}-Z_{LVp+1}}{Z_{p,R,SCi}} \quad (5$$	$$V_{j\to k,SCi}\big\vert_{i<j<k} = E_{DGj}\frac{1}{1+(jX_{DGj}/Z_{j,SCi})}\prod_{p=1}^{k-1}\frac{Z_{p,R,SCi}-Z_{LVp+1}}{Z_{p,R,SCi}} \quad (9$$
$$V_{j\to k,SCi}\big\vert_{k<j<i} = E_{DGj}\frac{1}{1+(jX_{DGj}/Z_{j,SCi})}\prod_{p=k+1}^{j}\frac{Z_{p,L,SCi}-Z_{LVp}}{Z_{p,R,SCi}} \quad (6$$	$$V_{j\to k,SCi}\big\vert_{i<k<j} = E_{DGj}\frac{1}{1+(jX_{DGj}/Z_{j,SCi})}\prod_{p=k+1}^{j}\frac{Z_{p,L,SCi}-Z_{LVp}}{Z_{p,R,SCi}} \quad (10$$
$$Z_{k,SCi} = Z_{k,L,SCi}//Z_{k,R,SCi}//Z_{Lk} \quad (11)$$	

Table II Objective function and constraints of optimization

Objective function	$$f(X_{DG},\ PL) = \left[\sum_{i=1}^{6}\sum_{j=1}^{6}\sum_{k=1}^{6} V_{jLVk,SC\_1LVi}\right](X_{DG},\ PL)$$
Constraints	$$OD_k < OD_{limit} \text{ at } k\text{-bus}$$

V. CONCLUSION

In this paper, the design aspects of low-voltage DG-PV units were investigated in order to comply with LVRTC requirements. The theoretical analysis revealed how the impedance of the DG units affects the bus voltages of the distribution network after a fault occurrence. Moreover, the concept of voltage selectivity is defined. Certainly, the DG-PV over-sizing has to be limited (up to 75 or 100%) so as to avoid an exaggerated power converter size and cost. In this direction, an optimum design for DG-PV units was proposed, concerning the maintenance of bus voltages of the low-voltage distribution network at the highest possible levels in case of a disturbance, achieving so voltage selectivity according to the LVRTC scheme. This optimisation process revealed that when the OD_{limit} relaxes (10–100%), then voltage selectivity may be attained under various PL values (considerably higher than the current ones), with minimum impact on the network protection settings. Therefore the present paper sets the necessary design challenges for the power electronics' designers, in terms of effective development of DG-PV converters suitable for increased PL values.

VI. ACKNOWLEDGEMENT

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VII. NOMENCLATURE

PL	penetration level (%)
PV	photovoltaic generator
lv (t)	the upstream equivalent single-phase network voltage source waveform (V)
LV	the vector representation of $lv(t)$ (pu)
DGk	distributed generator connected to k-bus
Z_{Lk}	the equivalent single-phase load impedance at k-bus ($k=1,2,.....n$) pu
X_{DGk}	the equivalent single-phase series reactance of LVDG-PV generation at k-bus (pu)
Z_S	the equivalent single-phase upstream network impedance calculated at the low voltage (LV) side of medium voltage/low voltage transformer (pu)
e_{DGk}	the equivalent single-phase AC voltage source time-function of LVDG-PV generation at k-bus (pu)
i	the short-circuited bus (i = 0, 1, …, n)
$Z_{k,L,\ SCi}$	the equivalent single-phase impedance at k-bus because of the upstream network in case of a three-phase short circuit at i-bus (pu)
$Z_{k,R,SCi}$	the equivalent single-phase impedance at k-bus because of the downstream network in case of a three-phase short circuit at i-bus (pu)
$Z_{k,SCi}$	the equivalent single-phase impedance at k-bus because of the total network in case of a three-phase short circuit at i-bus (pu)
E_{DGk}	the vector representation of e_{DGk} (pu)
P_{DGk}	the nominal active power injection of DGk at k-bus (pu)
I_{DGk}	the rms nominal phase current of DGk at steady state (pu)
$I_{DGk,SCi}$	the contribution to fault current vector of DGk at k-bus in case of a three-phase short circuit at i-bus (pu)
V_k	the nominal phase to ground voltage at k-bus (pu)
δ_k	the power angle between E_{DGk} and V_k (rad)
$V_{k,SCi}$	the voltage vector at k-bus in case of a three-phase short circuit at i-bus (pu)
$V_{k\rightarrow k,SCi}$	the voltage contribution vector of DGk at k-bus in case of a three-phase short circuit at i-bus (pu)
$i_{SC}(t)$	the short-circuit current waveform in case of a three-phase short circuit at i-bus (A)
ΣP_{DG}	the total generated active power of DG-PV units (W)
Σs_{LOAD}	the total load demand of the distribution network (KVA)
$V_{jLVk,\ SC\_1LVi}$	the rms-voltage value at jLVk-bus (j = 1, …, 6), (k = 1, …, 6) in case of a three-phase short circuit at i-bus (i = 1, …, 6) (pu)
$I_{DGk\text{-}tr}$	the maximum transient current capability of DGk converter during disturbances, equal to 2.8 times the I_{DGk}(pu)
d_k	the ratio of DGk converter over-dimensioning (OD) in relation to I_{DGk}
OD_k	the necessary over-dimensioning percentage of DGk converter in order to meet the LVRTC demands (%)
OD_{limit}	the optimisation constraint value of OD factor (%)
I_{SC}	the ratio of the bus short-circuit current in the examined network to the short-circuit current if there is not any installed DG in the network (pu)

VIII. APPENDIX

For $k < i$

$$\boldsymbol{Z}_{k,\mathrm{L,\,SC}i}\big|_{k<i} = \left[\left\{\left(\begin{array}{l}\{[(\boldsymbol{Z}_S+\boldsymbol{Z}_{\mathrm{LV1}})//\mathrm{j}X_{\mathrm{DG1}}//\boldsymbol{Z}_{\mathrm{L1}}]+\boldsymbol{Z}_{\mathrm{LV2}}\}\\ //\mathrm{j}X_{\mathrm{DG2}}//\boldsymbol{Z}_{\mathrm{L2}}\end{array}\right)+\ldots\right\}+\boldsymbol{Z}_{\mathrm{LV}k-1}\right] //\mathrm{j}X_{\mathrm{DG}k-1}//\boldsymbol{Z}_{\mathrm{L}k-1}+\boldsymbol{Z}_{\mathrm{LV}k}$$

$$\boldsymbol{Z}_{k,R,\mathrm{SC}i}\big|_{k<i} = \left[\left(\left\{\begin{array}{l}[(\boldsymbol{Z}_{\mathrm{LV}i}//\mathrm{j}X_{\mathrm{DG}i-1}//\boldsymbol{Z}_{\mathrm{L}i-1})+\boldsymbol{Z}_{\mathrm{LV}i-1}]\\ //\mathrm{j}X_{\mathrm{DG}i-2}//\boldsymbol{Z}_{\mathrm{L}i-2}\end{array}\right\}+\ldots\right)+\boldsymbol{Z}_{\mathrm{LV}k+2}\right] //\mathrm{j}X_{\mathrm{DG}k+1}//\boldsymbol{Z}_{\mathrm{L}k+1}+\boldsymbol{Z}_{\mathrm{LV}k+1}$$

For $k > i$

$$Z_{k,\mathrm{L},\mathrm{SC}i}\big|_{k>i} = \left[\left\{\begin{array}{l}(Z_{\mathrm{LV}i+1}//\mathrm{j}X_{\mathrm{DG}i+1}//Z_{\mathrm{L}i+1} + Z_{\mathrm{LV}i+2}) \\ \quad //\mathrm{j}X_{\mathrm{DG}i+2}//Z_{\mathrm{L}i+2} + \ldots\end{array}\right\} + Z_{\mathrm{LV}k-1}\right] //\mathrm{j}X_{\mathrm{DG}k-1}//Z_{\mathrm{L}k-1} + Z_{\mathrm{LV}k}$$

$$Z_{k,R,\mathrm{SC}i}\big|_{k>i} = \left[\begin{array}{l}\{(Z_{\mathrm{L}n}//\mathrm{j}X_{\mathrm{DG}n} + Z_{\mathrm{LV}n})//Z_{\mathrm{L}n-1}//\mathrm{j}X_{\mathrm{DG}n-1} + Z_{\mathrm{LV}n-1}\} \\ \quad //\ldots + Z_{\mathrm{LV}k+2}\end{array}\right] //Z_{\mathrm{L}k+1}//\mathrm{j}X_{\mathrm{DG}k+1} + Z_{\mathrm{LV}k+1}$$

REFERENCES

[1]. Denholm, P., Margolis, R., Mai, T., *et al*.: 'Bright future: solar power as a major contributor to the U.S. grid', *IEEE Power Energy Mag*., 2013, 11, (2), pp. 22–32
[2]. von Appen, J., Braun, M., Stetz, T., Diwold, K., Geibel, D.: 'Time in the sun: the
[3]. challenge of high PV penetration in the German electric grid', *IEEE Power Energy Mag.*, 2013, 11, (2), pp. 55–64
[4]. Directive 2009/28/EC of the European Parliament and of the Council of 23 April 2009 on the promotion of the use of energy from renewable sources and amending and subsequently repealing Directives 2001/77/EC and 2003/30/EC
[5]. NREL: 'Non-hardware ('soft') cost-reduction roadmap for residential and small commercial solar photovoltaics, 2013–2020' (NREL Publications, Denver, USA, 2013)
[6]. Koutroulis, E., Blaabjerg, F.: 'Methodology for the optimal design of
[7]. transformerless grid-connected PV inverters', *IET Power Electron.*, 2012, 5, (8), pp. 1491–1499
[8]. Carbone, R., Tomaselli, A.: 'Recent advances on AC PV-modules for grid-connected photovoltaic plants'. 2011 Int. Conf. on Clean Electrical Power (ICCEP), Ischia, Italy, June 2011, pp. 124–129
[9]. Eltawil, M.A., Zhao, Z.: 'Grid-connected photovoltaic power systems: technical and potential problems – a review', *Elsevier Renew. Sust. Energy Rev.*, 2010, 14, (1), pp. 112–129
[10]. Hossain, M.J., Pota, H.R., Ramos, R.A.: 'Improved low-voltage-ride-through
[11]. capability of fixed speed wind turbines using decentralised control of STATCOM with energy storage system', *IET Gener. Trans. Distrib.*, 2012, 6, (8), pp. 719–730
[12]. Papaefthimiou, S., Papathanassiou, S., Papadopoulos, M.: 'Evaluation of voltage dips in autonomous island networks and correlation with wind turbine FRT curves'. Proc. CIRED'09, Prague, June 2009
[13]. Vidal, J., Abad, G., Arza, J., Aurtenechea, S.: 'Single-phase DC crowbar topologies for low voltage ride through fulfillment of high-power doubly fed induction generator-based wind turbines', *IEEE Trans. Energy Convers.*, 2013,
[14]. 28, (3), pp. 768–781

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