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An Enhancement Of A Grid-Connected Dual Voltage Source Inverter By Using Multilevel Inverter

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ABSTRACT: This paper shows a dual voltage source inverter (DVSI) plan to upgrade the power quality and dependability of the micro grid system. The proposed scheme is involved two inverters, which empowers the micro grid to trade power created by the distributed energy resources (DERs) furthermore to compensate the nearby unbalanced and nonlinear load. The control calculations are produced taking into account instantaneous symmetrical component theory (ISCT) to work DVSI in grid sharing and grid infusing modes. The extension plan has expanded to multilevel inverter compare to the main voltage source inverter (MVSI)

KEYWORDS: Grid-connected inverter, instantaneous symmetrical component theory (ISCT), microgrid, power quality, multilevel converter**.**

I. INTRODUCTION

TECHNOLOGICAL progress and ecological concerns drive the power system to an outlook change with additional renewable energy sources coordinated to the system by means of distributed generation (DG). These DG units with composed control of local generation and storage facilities micro grid [1]. In a micro grid, power from various renewable energy sources, for example, energy units, photovoltaic (PV) systems, what's more, wind energy systems are interfaced to grid and loads utilizing power electronic converters. A grid interactive inverter plays an important role in exchanging power from the micro grid to the grid and the connected load [2], [3]. This micro grid inverter can either work in a grid sharing mode while supplying a part of local load or in grid injecting mode, by injecting power to the main grid.

Keeping up power quality is another imperative perspective which must be tended to while the micro grid system is connected with the fundamental network. The expansion of power hardware gadgets what's more, electrical loads with lopsided nonlinear streams has debased the power quality in the power appropriation system. Additionally, if there is a lot of feeder impedance in the conveyance system, the proliferation of these symphonious streams bends the voltage at the point of common Coupling (PCC). At the same moment, industry computerization has come to an abnormal state of refinement, where plants like car assembling units, substance processing plants, and Semiconductor commercial ventures require clean power. For these applications, it is fundamental to compensation and power injection using grid interactive nonlinear and unbalanced load currents [4].

Load compensation and power injection using grid interactive inverters in micro grid have been displayed in the writing [5], [6]. A single inverter system with power quality upgrade is examined. The primary center of this work is to acknowledge double functionalities in an inverter that would give the active power from a solar PV system furthermore functions as a active power filter, repaying unbalances and the reactive power required by other loads connected to the system.

In [8], a voltage direction and power flow control scheme for a wind energy system (WES) is proposed. A distribution static compensator (DSTATCOM) is used for voltage direction furthermore for active power infusion. The control plan keeps up the power equalization at the framework terminal during the wind varieties utilizing sliding mode control. A multifunctional power electronic converter for the DG power system is described [9]. This plan has the ability to inject power created by WES furthermore to execute as a consonant compensator. The greater part of the reported writing here talk about the topologies and control calculations to give load remuneration ability in the same inverter not withstanding their active power infusion. At the point when a grid-connected inverter is utilized for active power injection and also for load compensation, the inverter limit that can be used for accomplishing the second target is chosen by the available immediate micro grid real power [10]. Considering the instance of a lattice connected PV inverter, the available limit of the inverter to supply the reactive power turns out to be less during the maximum solar insolation periods. At the same moment, the reactive power to regulate the PCC voltage is particularly required during this period. It shows that giving multifunctional ties in a single inverter corrupts either the real power injection or the load compensation capabilities.

II. DUAL VOLTAGE SOURCE INVERTER

A. System Topology

This paper exhibits a double voltage source inverter (DVSI) plan, in which the power produced by the micro grid is infused as real power by the fundamental voltage source inverter (MVSI) and the reactive, harmonic, and unbalanced load pay is performed by helper voltage source inverter (AVSI). This has favorable position that the evaluated limit of MVSI can simply be utilized to infuse genuine energy to the system, if adequate renewable power is available at the dc link. In the DVSI plan, as total load power is supplied by two inverters, power losses over the semiconductor switches of every inverter are lessened. This expands its unwavering quality when contrasted with a solitary inverter with multifunctional abilities. Additionally, littler size secluded inverters can work at high switching frequencies with a decreased size of interfacing inductor, the channel cost gets decreased. In addition, as the principle inverter is supplying real power, the inverter needs to track the basic positive arrangement of current. This decreases the data transfer capacity necessity of the principle inverter. The inverters in the proposed plan use two separate dc links. Since the helper inverter is supplying zero succession of load current, a three-stage three-leg inverter topology with a solitary dc stockpiling capacitor can be utilized for the fundamental inverter. This thusly diminishes the dc-join voltage prerequisite of the fundamental inverter.

Thusly, the powers produced from these sources utilize a power conditioning stage before it is connected to the contribution of MVSI. In this study, DER is being spoken to as a dc source. An inductor channel is utilized to take out the high-frequency switching parts created due to the switching of power electronic switches in the inverters. The system considered in this study is accepted to have some measure of feeder resistance Rg and inductance Lg. Due to the nearness of this feeder impedance, PCC voltage is influenced with sounds.

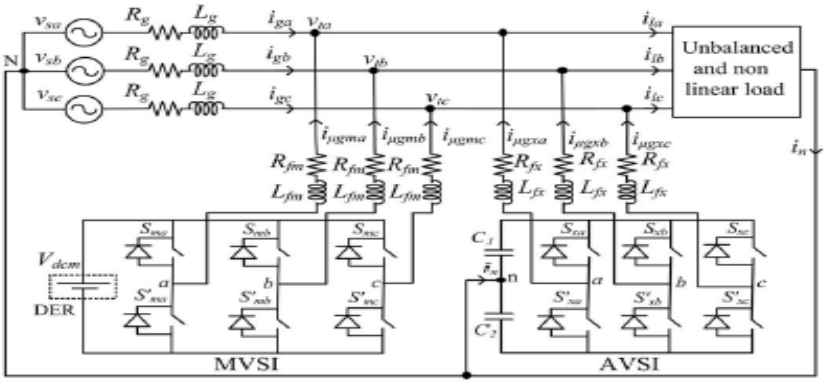


Fig. 1. Topology of proposed DVSI scheme.

Strategy for the reference current generation of two inverters in DVSI scheme.

B. Design of DVSI Parameters

1) AVSI: The vital parameters of AVSI like dc-connection voltage (Vdc), dc storage capacitors (C1 and C2), interfacing inductance (Lfx), and hysteresis band (±hx) are chosen based on the outline technique for split capacitor DSTATCOM topology. The dc-link voltage over every capacitor is taken as 1.6 times the top of stage voltage. The total dc-link voltage Reference (Vdcref) is observed to be 1040 V.

Estimations of dc capacitors of AVSI are picked taking into account the change in dc-link voltage during transients. Let complete load rating is S kVA. In the most pessimistic scenario, the load power may shift from least to most extreme, i.e., from 0 to S kVA. AVSI needs to trade real power during transient to keep up the load power request. This transfer of real power during the transient will bring about deviation of capacitor voltage from its reference value. Accept that the voltage controller takes n cycles, i.e., nT seconds to act, where T is the system day and age. Consequently, most extreme energy trade by AVSI during transient will be nST. This energy will be equivalent to change in the capacitor put away energy. Accordingly

$$\frac{1}{2}C_1(V_{\mathrm{dcr}}^2 - V_{\mathrm{dc1}}^2) = nST \qquad (1)$$

Where Vdcr and Vdc1 are the reference dc voltage and maximum permissible dc voltage across C1 during transient, respectively. Here, S =5 kVA, Vdcr = 520 V, Vdc1 = 0.8 Vdcr or 1.2 Vdcr, n = 1, and T = 0.02 s. Substituting these values in (1), the dc link capacitance (C1) is calculated to be 2000 μF. Same value of capacitance is selected for C2. The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,h_x f_{\max}}. \qquad (2)$$

C. Advantages of the DVSI Scheme

The different preferences of the proposed DVSI plan over a single inverter plan with multifunctional capacities are examined here as takes after:

1) **Increased Reliability**: DVSI plan has expanded dependability, because of the decrease in disappointment rate of segments and the decrease in system down time cost. In this plan, the all out load current is shared amongst AVSI and MVSI and henceforth diminishes the disappointment rate of inverter switches. In addition, in the event that one inverter comes up short, the other can proceed with its operation. This decreases the lost energy and subsequently the down time cost. The lessening in system down time cost enhances the unwavering quality.

2) **Reduction in Filter Size**: In DVSI plan, the current supplied by every inverter is decreased and thus the present rating of individual channel inductor decreases. This decrease in current rating decreases the channel size. Additionally, in this plan, hysteresis current control is utilized to track the inverter reference currents. As given in (2), the channel inductance is chosen by the inverter switching frequency. Since the lower current evaluated semiconductor device can be exchanged at higher switching frequency, the inductance of the channel can be brought down. This decrease in inductance further diminishes the channel size.

3) **Improved Flexibility**: Both the inverters are nourished from separate dc links which permit them to work freely, consequently expanding the adaptability of the system. Case in point, if the dc connection of the principle inverter is detached from the system, the load pay ability of the assistant inverter can in any case be used.

4) **Better Utilization of Micro grid Power**: DVSI plan uses full limit of MVSI to exchange the whole power produced by DG units as real power to ac bus, as there is AVSI for symphonious and reactive power remuneration. This builds the active power infusion ability of DGs in micro grid.

5) **Reduced DC-Link Voltage Rating**: Since, MVSI is most certainly not conveying zero succession load current parts; a solitary capacitor three-leg VSI topology can be utilized. In this way, the dc link voltage rating of MVSI is decreased around by 38%, when contrasted with a single inverter system with split capacitor VSI topology.

III. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control calculation for reference current generation using ISCT requires adjusted sinusoidal PCC voltages. As a result of the nearness of feeder impedance, PCC voltages are misshaped. In this manner, the key positive grouping segments of the PCC voltages are separated for the reference current generation. To change over the mutilated PCC voltages to balanced

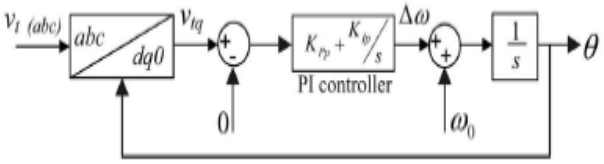


Fig. 2. Schematic diagram of PLL.

Sinusoidal voltages, dq0 transformation are used. The PCC voltages in natural reference frame (vta, vtb, and vtc) are first transformed into dq0 reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \qquad (3)$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

So as to get θ, an altered synchronous reference outline (SRF) phase locked loop (PLL) is utilized. The schematic outline of this PLL is appeared in Fig. 2. It for the most part comprises of a proportional integral (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-pivot (vtq) is contrasted and 0 V what's more, the mistake voltage in this way got is given to the PI controller. The frequency deviation Δω is then added to the reference frequency ω0 lastly given to the integrator to get θ. It can be demonstrated that, when, θ = ω0 t and by utilizing the Park's change system(C), q-pivot voltage in dq0 outline gets to be zero and thus the PLL will be bolted to the reference frequency (ω0). As PCC voltages are mutilated, the changed voltages in dq0 outline (vtd and vtq) contain normal and wavering segments of voltages. These can be spoken to as

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td}, \quad v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \qquad (4)$$

Where vtd and vtq speak to the normal segments of vtd and vtq, separately. The terms $\widetilde{v}_{td}$ and $\widetilde{v}_{tq}$ show the swaying segments of vtd and vtq, separately. Presently the principal positive sequence of PCC voltages in normal reference frame can be acquired with the assistance of opposite dq0 change as given by

$$\begin{bmatrix} v_{ta1}^{+} \\ v_{tb1}^{+} \\ v_{tc1}^{+} \end{bmatrix} = C^{T} \begin{bmatrix} \overline{v}_{td} \\ \overline{v}_{tq} \\ 0 \end{bmatrix}. \qquad (5)$$

These voltages v+ ta1, v+ tb1, and v+ tc1 are utilized as a part of the reference current generation calculations, in order to draw adjusted sinusoidal currents from the grid.

B. Instantaneous Symmetrical Component Theory

ISCT was produced basically for unbalanced and nonlinear load pay by active power filters. The system topology appeared in Fig. 3 is utilized for understanding the reference current for the compensator. The ISCT for load compensation is inferred in light of the accompanying three conditions.

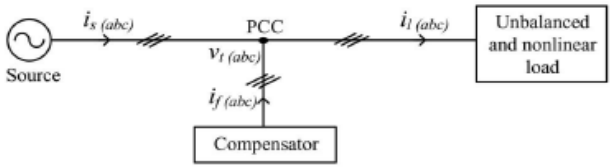


Fig. 3. Schematic of an unbalanced and nonlinear load compensation scheme

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0. \qquad (6)$$

2) The phase angle between the fundamental positive sequence voltage (v+ ta1) and source current (isa) is φ

$$\angle v_{ta1}^{+} = \angle i_{sa} + \phi. \qquad (7)$$

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta1}^{+} i_{sa} + v_{tb1}^{+} i_{sb} + v_{tc1}^{+} i_{sc} = P_l. \qquad (8)$$

Solving the above three equations, the reference source currents can be obtained as

$$\begin{aligned} i_{sa}^{*} &= \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \\ i_{sb}^{*} &= \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{ta1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \\ i_{sc}^{*} &= \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \end{aligned} \qquad (9)$$

Where $\beta = \frac{\tan\phi}{\sqrt{3}}$ the term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute β = 0in (9). Thus, the reference source currents for three phases are given by

$$i_{s(abc)}^{*} = \left(\frac{v_{t(abc)1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \qquad (10)$$

Where i∗sa, i∗sb, and i∗sc are principal positive succession of load streams drawn from the source, when it is supplying a normal load power Pl. The power Pl can be processed utilizing a moving normal channel with a window of one-cycle information focuses as given below

$$P_l = \frac{1}{T} \int_{t_1 - T}^{t_1} (v_{ta1}^{+} i_{la} + v_{tb1}^{+} i_{lb} + v_{tc1}^{+} i_{lc}) dt \qquad (11)$$

Where *t*1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i_{f\,(abc)}^{*} = i_{l\,(abc)} - i_{s\,(abc)}^{*}. \qquad (12)$$

Equation (12) can be utilized to produce the reference channel currents utilizing ISCT, when the whole load active power, Pl is supplied by the source and load pay is performed by a solitary inverter. A change in the control calculation is required, when it is utilized for DVSI plan. The accompanying area talks about the detailing of control calculation for DVSI plan.

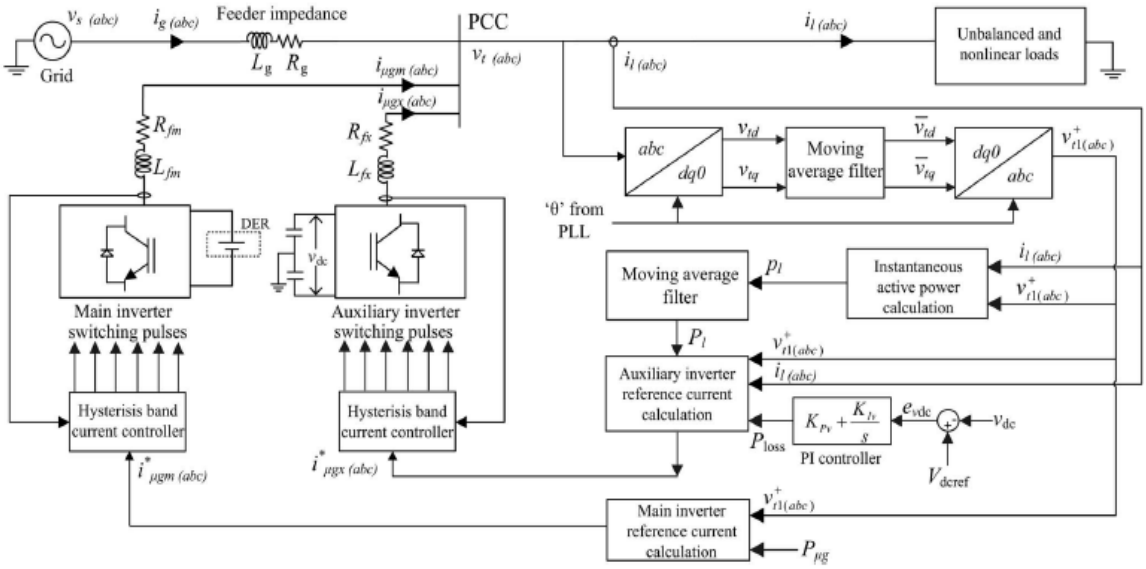


Fig. 4. Schematic diagram showing the control strategy of proposed DVSI scheme.

C. Control Strategy of DVSI

Control system of DVSI is produced in a manner that grid and MVSI together share the active load power, and AVSI supplies rest of the power segments requested by the load.

1) Reference Current Generation for Auxiliary Inverter:

The dc-link voltage of the AVSI ought to be looked after steady for appropriate operation of the helper inverter. DC-link voltage variety happens in helper inverter because of its switching and ohmic losses. These losses termed as Ploss ought to likewise be supplied by the grid. An expression for Ploss is inferred on the condition that normal dc capacitor current is zero to keep up a steady capacitor voltage. The deviation of normal capacitor current from zero will reflect as an adjustment in capacitor voltage from a steady state value. A PI controller is utilized to produce Ploss term as given by

$$P_{\text{loss}} = K_{Pv}\, e_{\text{vdc}} + K_{Iv} \int e_{\text{vdc}}\, dt \qquad (13)$$

Where evdc = Vdcref − vdc, vdc speaks to the real voltage detected and upgraded once in a cycle. In the above condition, KPv furthermore, KIv speak to the relative and vital increases of dc-connection PI controller, separately. The Ploss expression hence got ought to be supplied by the lattice, and hence AVSI reference currents can be gotten as given in (14). Here, the dc-link voltage PI controller additions are chosen in order to guarantee soundness and better dynamic reaction during load change.

$$\begin{aligned} i^*_{\mu gxa} &= i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\ i^*_{\mu gxb} &= i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\ i^*_{\mu gxc} &= i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}). \end{aligned} \qquad (14)$$

2) Reference Current Generation for Main Inverter:

The MVSI supplies adjusted sinusoidal currents in view of the available renewable power at DER. On the off chance that MVSI losses are dismissed, the power infused to system will be equivalent to that available at DER (Pμg). The accompanying condition, which is gotten from ISCT can be utilized to produce MVSI reference currents for three phases (a, b, and c)

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) P_{\mu g} \qquad (15)$$

Where Pμg is the accessible power at the dc connection of MVSI. The reference currents acquired from (14) to (15) are followed by utilizing hysteresis band current controller (HBCC). HBCC plans depend on an input loop, generally with a two-levelcomparator. This controller has the advantage of peak current constraining limit, good dynamic response, and straightforwardness in usage. A hysteresis controller is a high-increase corresponding controller. This controller includes certain phase lag in the operation in view of the hysteresis band and won't make the system temperamental. Likewise, the proposed DVSI plan utilizes a initially arrange

inductor channel which retains the closed-loop system strength. The whole control procedure is schematically spoken to in Fig. 4. Applying Kirchhoff's present law (KCL) at the PCC in Fig. 4

$$i_{\mu g x\, j} = i_{l\, j} - (i_{g\, j} + i_{\mu g m\, j}), \quad \text{for } j = a, b, c. \qquad (16)$$

By using (14) and (16), an expression for reference grid current in phase-*a* (i^*_{ga}) can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)[(P_l + P_{\text{loss}}) - P_{\mu g}]. \qquad (17)$$

It can be watched that, if the amount (Pl + Ploss) is greater than Pµg, the term [(Pl + Ploss) − Pµg] will be a positive amount, what's more, i∗ga will be in stage with v+ ta1. This operation can be called as the system supporting or grid sharing mode, as the total load power interest is shared between the principle inverter and the system. The term, Ploss is generally little contrasted with Pl. Then again, if (Pl + Ploss) is not exactly Pµg, then [(Pl + Ploss) − Pµg] will be a negative amount, and consequently i∗ga will be in phase restriction with v+ ta1. This method of operation is called the network infusing mode, as the excess power is injected to grid.

D. Multilevel Converter

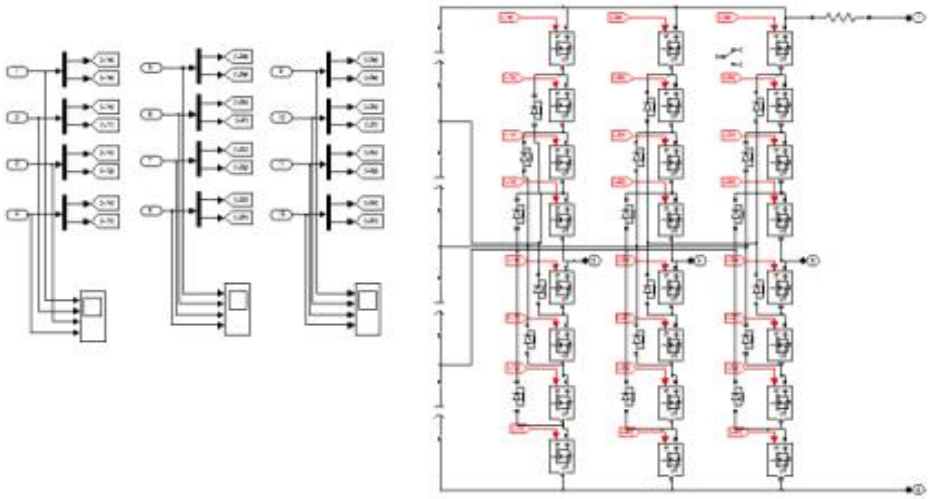


Fig.5.diode clamped multilevel inverter

Various modern applications have started to require higher power mechanical assembly as of late. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect one and only power semiconductor switch straightforwardly. Accordingly, a multilevel power converter structure has been presented as an option in high power and medium voltage circumstances. A multilevel converter accomplishes high power evaluations, as well as empowers the utilization of renewable energy sources. Renewable energy sources, for example, photovoltaic, wind, and energy components can be effortlessly interfaced to a multilevel converter system for a powerful application.

The term multilevel started with the three-level converter. Consequently, a few multilevel converter topologies have been produced. Nonetheless, the rudimentary idea of a multilevel converter to accomplish higher power is to utilize a progression of power semiconductor switches with a few lower voltage dc sources to play out the power change by incorporating a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be utilized as the different dc voltage sources. The replacement of the power switches total these different dc sources so as to accomplish high voltage at the output; be that as it may, the appraised voltage of the power semiconductor switches depends just upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has a few points of interest over a customary two-level converter that utilizations high switching frequency beat width regulation (PWM). The appealing elements of a multilevel converter can be quickly abridged as takes after.

● Staircase waveform quality: Multilevel converters not just can produce the output voltages with low mutilation additionally can diminish the dv/dt stresses; thusly electromagnetic similarity (EMC) issues can be lessened.

● Common-mode (CM) voltage: Multilevel converters produce littler CM voltage; hence, the anxiety in the heading of a motor connected with a multilevel engine drive can be decreased. Besides, CM voltage can be killed by utilizing propelled tweak procedures, for example, that proposed.

- Input current: Multilevel converters can draw info current with low contortion.
- Switching frequency: Multilevel converters can work at both essential switching frequency and high switching frequency PWM. It ought to be noticed that lower switching frequency for the most part means lower switching loss and higher effectiveness.

E. Diode Clamped Multilevel Inverter:

The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels. This type of inverters provides the high efficiency because the fundamental frequency used for all the switching devices and it is a simple method of the back to back power transfer systems.

Ex: 5- Level diode clamped multilevel inverter,

- The 5- level diode clamped multilevel inverter uses switches, diodes; a single capacitor is used, so output voltage is half of the input DC.

Shockingly, multilevel converters do have a few impediments. One specific inconvenience is the more prominent number of power semiconductor switches required. In spite of the fact that lower voltage appraised switches can be used in a multilevel converter, every switch requires a related door drive circuit. Copious multilevel converter topologies have been proposed during the most recent two decades. Contemporary examination has drawn in novel converter topologies and exceptional regulation plans. In addition, three diverse major multilevel converter structures have been accounted for in the writing: fell H-bridge converter with partitioned dc sources, diode cinched (nonpartisan braced), and flying capacitors (capacitor clipped). In addition, plentiful balance strategies and control ideal models have been produced for multilevel converters, for example, sinusoidal heartbeat width regulation (SPWM), particular symphonious disposal (SHE-PWM), space vector tweak (SVM), and others. What's more, numerous multilevel converter applications concentrate on modern medium-voltage motor drives, utility interface for renewable energy systems, adaptable AC transmission system (FACTS), and footing drive systems.

IV. SIMULATION RESULTS

The simulation model of DVSI scheme shown in Fig. 1 is developed in PSCAD 4.2.1 to evaluate the performance. The simulation parameters of the system are given in Table I. The simulation study demonstrates the grid sharing and grid injecting modes of operation of DVSI scheme in steady state as well as in transient conditions. The distorted PCC voltages due to the feeder impedance without DVSI scheme are shown in Fig. 6(a). If these distorted voltages are used for the reference current generation of AVSI, the current compensation will not be proper [14].

Therefore, the fundamental positive sequence of voltages is extracted from these distorted voltages using the algorithm explained in Section III-A. These extracted voltages are given in Fig. 6(b). These voltages are further used for the generation of inverter reference currents. Fig. 7(a)–(d) represents active power demanded by load (*Pl*), active power supplied by grid (*Pg*), active power supplied by MVSI (*Pμg*), and active power supplied by AVSI (*Px*), respectively. It can be observed that, from $t = 0.1$ to 0.4 s, MVSI is generating 4 kW power and the load demand is 6 kW. Therefore, the remaining load active power (2 kW) is drawn from the grid. During this period, the microgrid is operating in grid sharing mode. At $t = 0.4$ s, the microgrid power is increased to 7 kW, which is more than the load demand of 6 kW. This microgrid power change is considered to show the change of operation of MVSI from grid sharing to grid injecting mode. Now, the excess power of 1 kW is injected to the grid and hence, the power drawn from grid is shown as negative. Fig. 8(a)–(c) shows the load reactive power (*Ql*), reactive power supplied by AVSI (*Qx*), and reactive power supplied by MVSI (*Qμg*), respectively. It shows that total load reactive power is supplied by AVSI, as expected.

Fig. 9(a)–(d) shows the plots of load currents (*il*(*abc*)), currents drawn from grid (*ig*(*abc*)), currents drawn from MVSI (*iμg*(*abc*)), and currents drawn from the AVSI (*iμx*(*abc*)), respectively. The load currents are unbalanced and distorted. The MVSI supplies a balanced and sinusoidal currents during grid supporting and grid injecting modes. The currents drawn from grid are also perfectly balanced and sinusoidal, as the auxiliary inverter compensates the unbalance and harmonics in load currents. Fig. 10(a) shows the plot of fundamental positive sequence of PCC voltage (*v+ta*1) and grid current in phase-*a* (*iga*) during grid sharing and grid injecting modes. During grid sharing mode, this PCC voltage and grid current are in phase and during grid injecting mode, they are out of phase. Fig. 10(b) establishes that MVSI current in phase-*a* is always in phase with fundamental positive sequence of phase-*a* PCC voltage. The same is true for other two phases. Thus the compensation capability of AVSI makes the source current and MVSI current at unity power factor operation.

The dc-link voltage of AVSI is shown in Fig. 11(a) and (b). These figures indicate that the voltage is maintained constant at a reference voltage (*V*dcref) of 1040 V by the PI controller. All these simulation results presented above demonstrate the feasibility of DVSI for the load compensation as well as power injection from DG units in a microgrid.

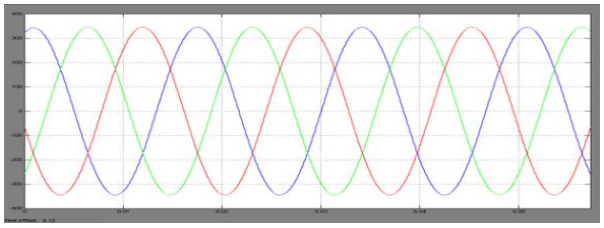


Fig. 6. Without DVSI scheme: (a) PCC voltages

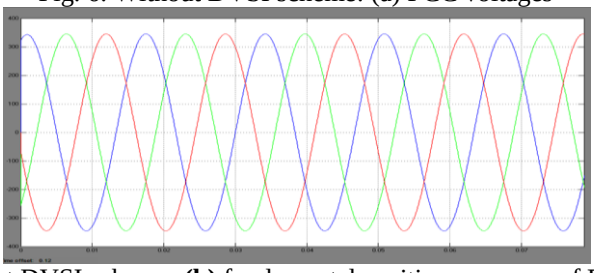


Fig. 6. Without DVSI scheme: **(b)** fundamental positive sequence of PCC voltages.

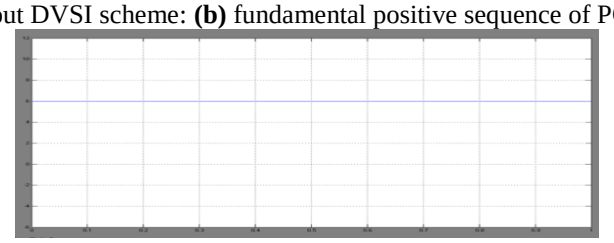


Fig. 7. Active power sharing: (a) load active power;

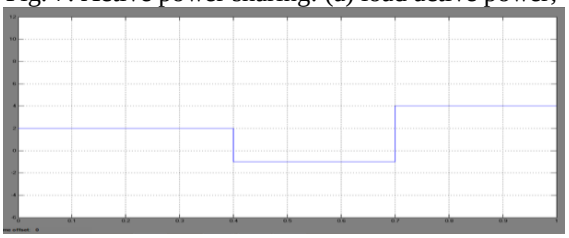


Fig. 7. Active power sharing: (b) active power supplied by grid;

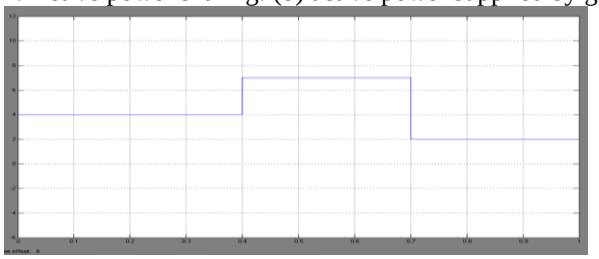


Fig. 7. Active power sharing: (c) active power supplied by MVSI;

Fig. 7. Active power sharing: (d) active power supplied by AVSI.

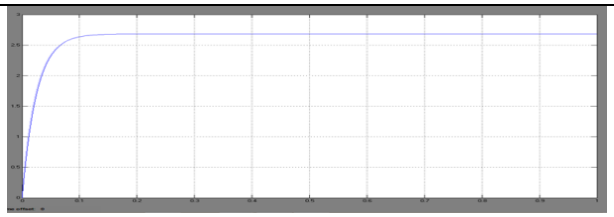


Fig. 8. Reactive power sharing: (a) load reactive power

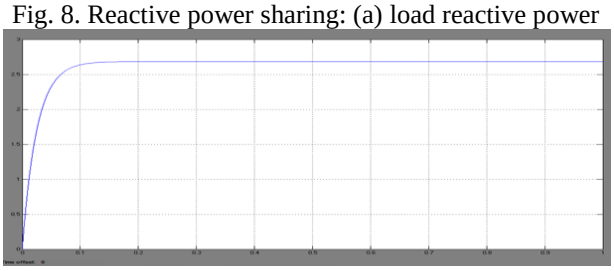


Fig. 8. Reactive power sharing: (b) reactive power supplied by AVSI;

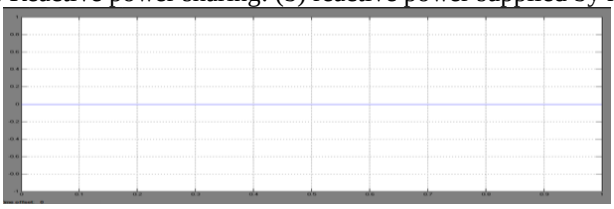


Fig. 8. Reactive power sharing: (c) reactive power supplied by MVSI.

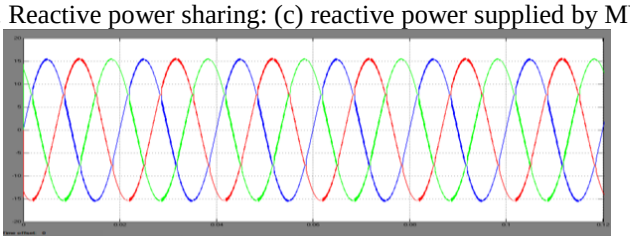


Fig. 9. Simulated performance of DVSI scheme: (a) load currents;

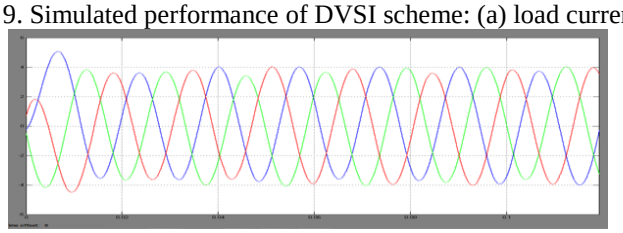


Fig. 9. Simulated performance of DVSI scheme: (b) grid currents;

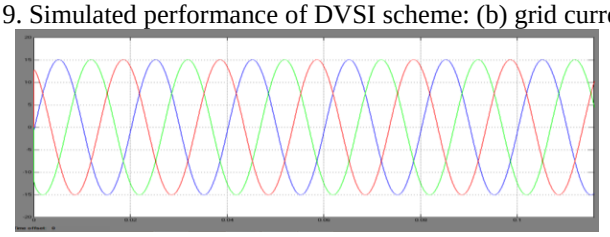


Fig. 9. Simulated performance of DVSI scheme: (c) MVSI currents;

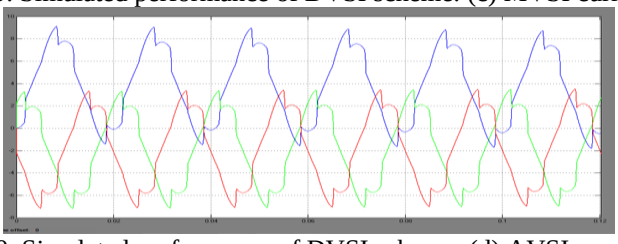


Fig. 9. Simulated performance of DVSI scheme: (d) AVSI currents.

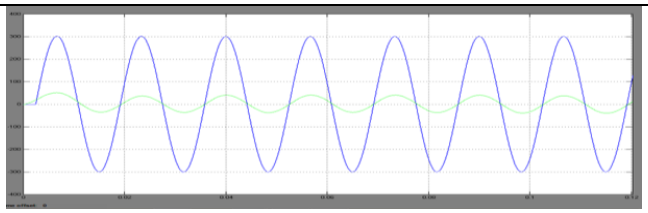


Fig. 10. Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-*a*)

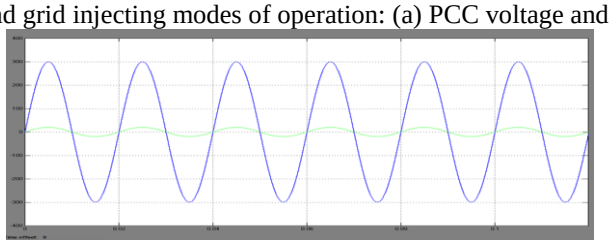


Fig. 10. Grid sharing and grid injecting modes of operation: (b) PCC voltage and MVSI current (phase-*a*).

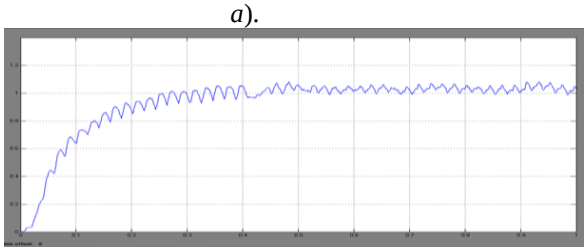


Fig. 11. (a) DC-link voltage of AVSI and (b) zoomed view of dc-link voltage dynamics during load change.

Extension results

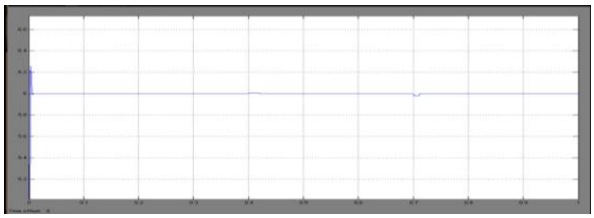


Fig. 12. Active power sharing: (a) load active power;

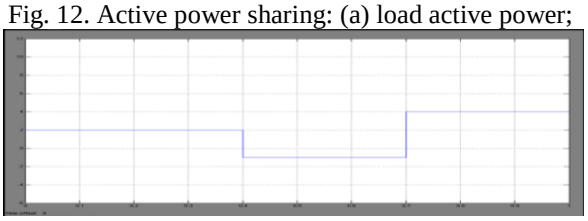


Fig. 12. Active power sharing: (b) active power supplied by grid;

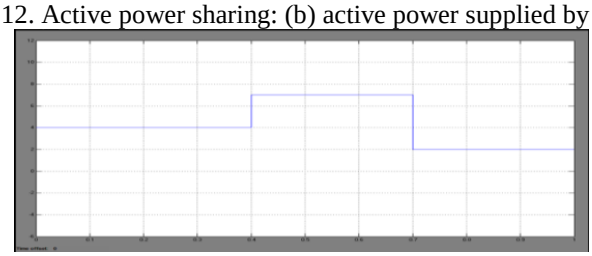


Fig. 12. Active power sharing: (c) active power supplied by MVSI;

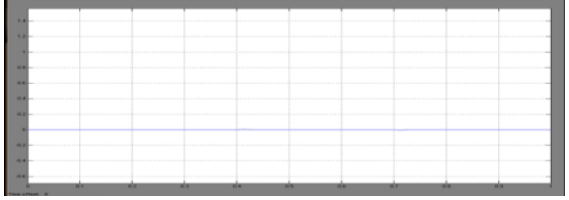


Fig. 12. Active power sharing: (d) active power supplied by AVSI.

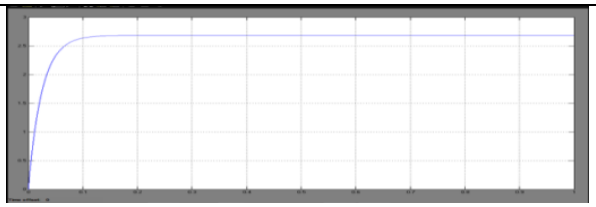


Fig. 13. Reactive power sharing: (a) load reactive power

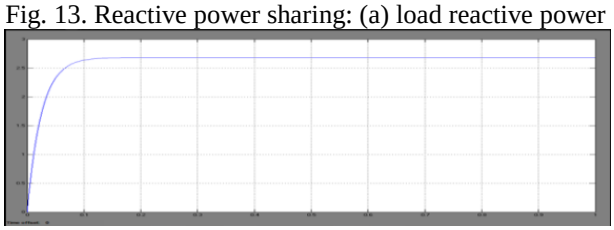


Fig. 13. Reactive power sharing: (b) reactive power supplied by AVSI;

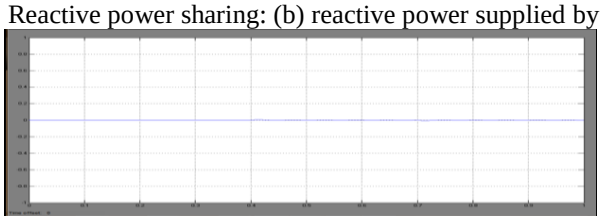


Fig. 13. Reactive power sharing: (c) reactive power supplied by MVSI.

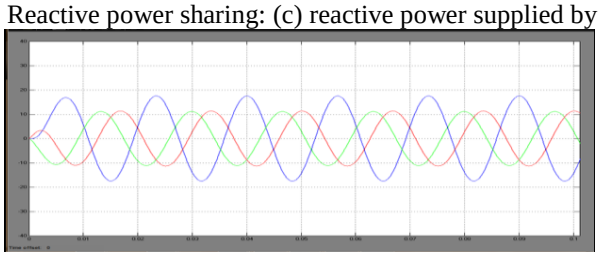


Fig. 14. Simulated performance of DVSI scheme: (a) load currents;

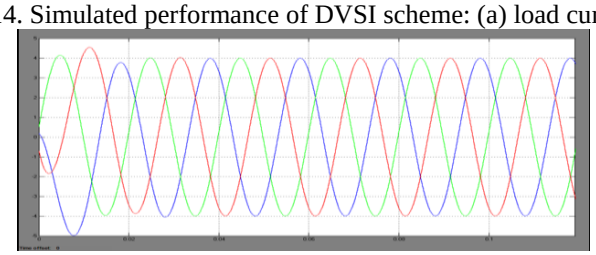


Fig. 14. Simulated performance of DVSI scheme: (b) grid currents;

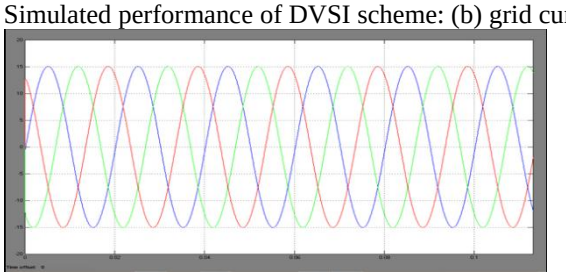


Fig. 14. Simulated performance of DVSI scheme: (c) MVSI currents;

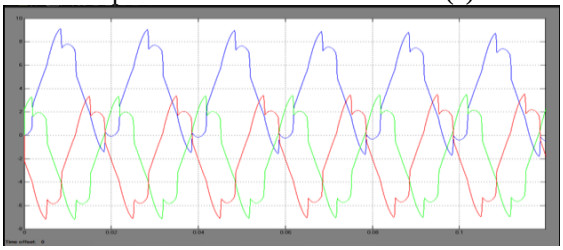


Fig. 14. Simulated performance of DVSI scheme: (d) AVSI currents.

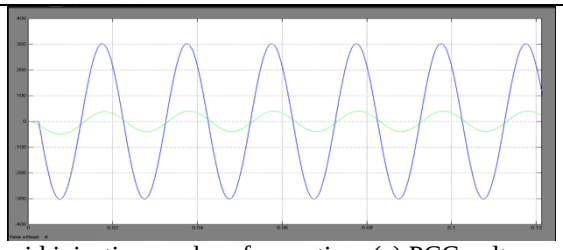


Fig. 15. Grid sharing and grid injecting modes of operation: (a) PCC voltage and grid current (phase-*a*)

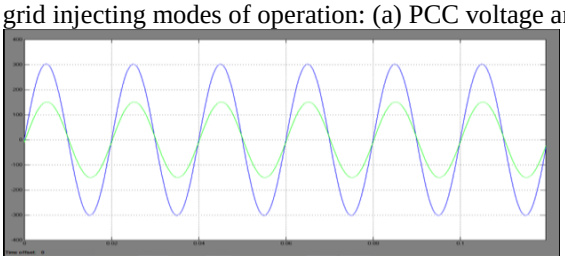


Fig. 15. Grid sharing and grid injecting modes of operation: (b) PCC voltage and MVSI current (phase-*a*).

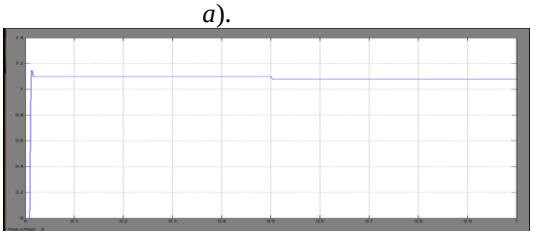


Fig. 16. (a) DC-link voltage of AVSI and (b) zoomed view of dc-link voltage dynamics during load change.

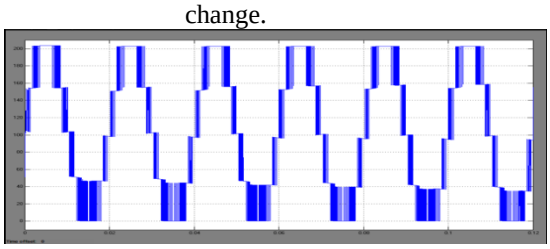
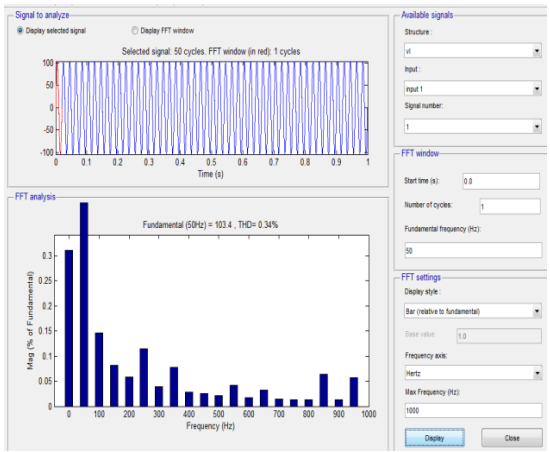


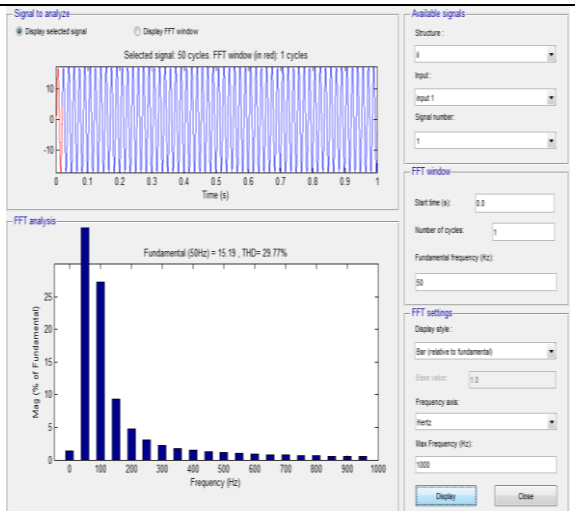
Fig.17.Five Level Output

V. COMPARISON

Extensiion results

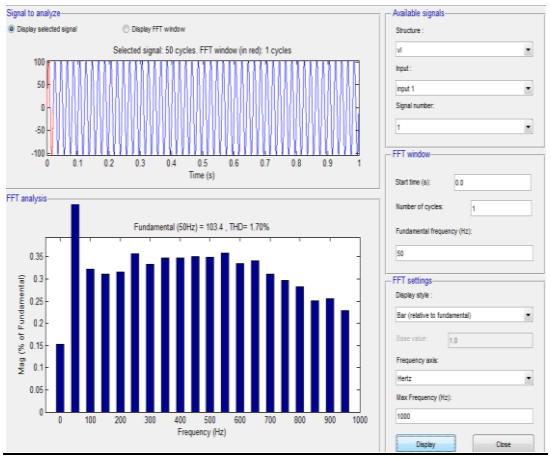


THD of the Load voltage

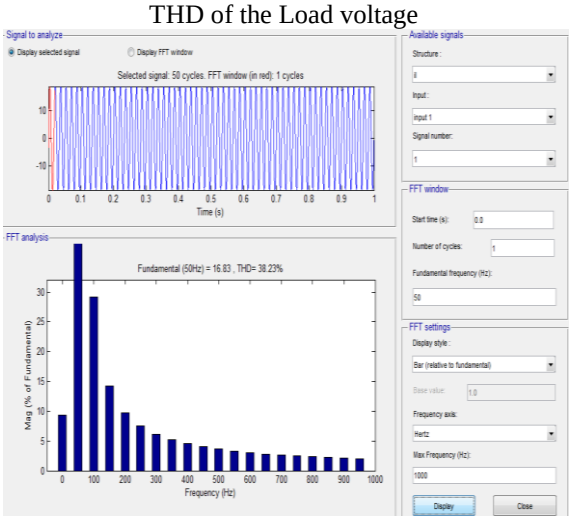


THD of the Load current

Proposed Results



THD of the Load voltage



THD of the Load current

Comparison Table of the THD of the Load voltage and Load current between proposed and extension Methods

TABLE.1

System Parameters	**Proposed Method** (total harmonic distortion)	**Extension Method** (total harmonic distortion)
Load Voltage	1.70%	0.34%
Load Current	38.23%	29.77%

From the above Table.1 it is clear that the total harmonic distortion (THD) will be reduced compared to proposed method and extension method that is the load voltage in proposed method is 1.70% that is reduced to 0.34% in extension method likewise the load current in proposed method is 38.23% that is also reduced to 29.77% because of the we use multi level (5Level) inverter in place of the MVSI inverter. We use multilevel inverter in place of normal inverter we increase number of levels because of that reason we get reduced THD in multilevel inverter we get low THD that means we get proper sine wave in inverter output. Because these reason we use multilevel inverters in place of normal inverters.

VI. CONCLUSION

A DVSI plan is proposed for micro grid systems with upgraded power quality. Control calculations are produced to create reference streams for DVSI utilizing ISCT. The proposed plan has the ability to trade power from disseminated generators (DGs) furthermore to repay the nearby unequal also, nonlinear load. The execution of the proposed plan has been approved through recreation and test thinks about. When contrasted with a single inverter with multifunctional capacities, a DVSI has numerous favorable circumstances, for example, expanded unwavering quality, lower cost because of the decrease in channel size, and more usage of inverter ability to infuse real power from DGs to micro grid. In DVSI, the use of multilevel inverter of the capacitors can be pre-charged as a group. Efficiency is high for fundamental frequency switching. Total harmonic distortion will be decreased.

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