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Grid Voltage Synchronization for Distributed Generation Systems Under Grid Fault Conditions

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ABSTRACT : The actual grid code requirements for the grid connection of distributed generation systems, mainly wind and photovoltaic (PV) systems, are becoming very demanding. The transmission system operators (TSOs) are especially concerned about the low-voltage-ride-through requirements. Solutions based on the installation of STATCOMs and dynamic voltage regulators (DVRs), as well as on advanced control functionalities for the existing power converters of distributed generation plants, have contributed to enhance their response under faulty and distorted scenarios and, hence, to fulfill these requirements. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algo- rithms, which are able to work under unbalanced and distorted conditions. This paper analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. In the following, the different algorithms will be pre- sented and discretized, and their performance will be tested in an experimental setup controlled in order to evaluate their accuracy and implementation features.

KEYWORDS – Photovoltaic, TSO, STATCOM, DVR, PLL

I. INTRODUCTION

The power share of renewable energy-based generation sys- tems is supposed to reach 20% by 2030, where wind and photovoltaic (PV) systems are assumed to be the most outstand- ing examples of integration of such systems in the electrical network [1].

The increased penetration of these technologies in the electri- cal network has reinforced the already existing concern among the transmission system operators (TSOs) about their influence in the grid stability; as a consequence, the grid connection stan- dards are becoming more and more restrictive for distribution generation systems in all countries [2]–[6].

In the actual grid code requirements (GCRs), special con- straints for the operation of such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand. Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic [7].

Although the LVRT requirements in the different standards are very different, as shown in [8], the first issue that generation systems must afford when a voltage sag occurs is the limitation of their transient response, in order to avoid its protective discon- nection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel cage induction generators, where the voltage drop in the stator windings can conduct the generator to an overspeed tripping, as shown in [9]. Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions [10], [11]. Likewise, PV systems would also be affected by the same lack of current controllability.

Solutions based on the development of auxiliary systems, such as STATCOMs and dynamic voltage regulators (DVRs), have played a decisive role in enhancing the fault ride through (FRT) capability of distributed generation systems, as demon- strated in [12]–[16]. Likewise, advanced control functionalities for the power converters have also been proposed [17], [18]. In any case, a fast detection of the fault contributes to improving the effects of these solutions; therefore, the synchronization algorithms are crucial.

In certain countries, the TSOs also provide the active/reactive power pattern to be injected into the network during a voltage sag; this is the case for the German E-on [2] and the Spanish Red Eléctrica Española (REE) [3]. This trend has been followed by the rest of the TSOs; moreover, it is believed that this operation

requirement will be extended, and specific demands for balanced and unbalanced sags will arise in the following versions of the grid codes worldwide [19].

Regarding the operation of the distributed generation systems under balanced and unbalanced fault conditions, relevant con- tributions, such as [20]–[29], can be found in the literature. These solutions are based on advanced control systems that need to have accurate information of the grid voltage variables in order to work properly, something that has prompted the im- portance of grid synchronization algorithms. In power systems, the synchronous reference frame PLL (SRF PLL) is the most extended technique for synchronizing with three-phase systems [30]. Nevertheless, despite the fact that the performance of SRF PLL is satisfactory under balanced conditions, its response can be inadequate under unbalanced, faulty, or distorted conditions [31]–[33].

In this paper, three improved and advanced grid synchroniza- tion systems are studied and evaluated: the decoupled double synchronous reference frame PLL (DDSRF PLL) [34], the dual second order generalized integrator PLL (DSOGI PLL), [35] and the three-phase enhanced PLL (3phEPLL) [36]. Their per- formance, computational cost, and reliability of the amplitude and phase detection of the positive sequence of the voltage, under unbalanced and distorted situations, have been evaluated according to experimental grid fault patterns extracted from [37] and [38], which have been reproduced in a real scaled electrical network.

In the following sections, the discrete representation of each PLL will be detailed (see Section IV), due to its great impor- tance in the final implementation of the control, after a brief description of the different structures (see Section III). Finally, their behavior will be tested in an experimental setup (see Section VI), and their performance will be discussed, partic- ularly taking into account the accuracy of the positive-sequence detection and their computational cost (see Section VII) when considering different faulty scenarios, covering the response in front of sags, frequency changes, and harmonic immunity.

II. HEADINGS

2. Grid Synchronization Specifications Based on GCR
3. Description of the Three Phase Systems
4. Discrete Implementation
5. Testing signals & Experimental Setup
6. Experimental Performance of the PLLs under Test
7. Evaluation of the Computational Burden Time

III. INDENTATIONS AND EQUATIONS

1. Grid Synchronization Specifications Based on GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on ana- lyzing the individual dynamic performance of each proposal, without first determining a time response window within the dynamic behavior of the system under test, which would be considered to be satisfactory.

In this paper, in order to evaluate the response of the grid synchronization topologies under test, a common performance requirement for all the structures has been established in this section, considering the needs that can be derived from the LVRT requirements.

Despite the fact that the detection of the fault can be carried out with simpler algorithms, as shown in [39] and [40], the importance of advanced grid synchronization systems lies in the necessity of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power required by the TSO.

In the German standard [2], it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the generator transformer to at least 2% of the rated current for each percent of the voltage dip, as shown in Fig. 1. 100% reactive power delivery must be possible, if necessary.

A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and be able to inject full reactive power after 150 ms, as shown in Fig. 2.

Considering these demands, this paper will consider that the estimation of the voltage conditions will be carried out within 20–25 ms, as this target permits it to fulfill the most restrictive requirements, in terms of dynamical response, available in the grid codes. This condition will be extended to frequency estimation; although this parameter is more related to secondary control algorithms than LVRT, the same time window between 20 and 25 ms will be considered in this work for the detection of the disturbance.

2. Description of the Three Phase Systems

Many of the positive-sequence detection algorithms are based on SRF PLLs [32]. Despite having a good response under balanced conditions, their performance becomes insufficient in unbalanced faulty grids (95% of cases), and their good opera- tion is highly conditioned to the frequency stability, which is incompatible with the idea of a robust synchronization system. Many authors have discussed different advanced models, which are able to overcome the problems of the classical PLL, using frequency and amplitude adaptive structures which are able to deal with unbalanced, faulty, and harmonic-polluted grids. In the framework of these topologies, three PLL structures will be discussed and evaluated in this paper.

A. DDSRF PLL

The DDSRF PLL, published in [34] and [41], was developed for improving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counterclockwise and another one clockwise, in order to achieve an accurate detection of the positive- and negative-sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF PLL is shown in Fig. 3.

When the three-phase grid voltage is unbalanced, the funda- mental positive-sequence voltage vector appears as a dc voltage on the dq^{+1} axes of the positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the dq^{-1} axes of the negative-sequence SRF. In contrast, the negative-sequence voltage vector will cause a dc component on the negative-sequence SRF and an ac oscillation on the positive- sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches the dc level on the negative- sequence SRF and vice versa, a decoupling network is applied to signals on the *dq* positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters (LPFs) in Fig. 3 are responsible for extracting the dc component from the signal on the decoupled SRF axes. These dc components collect information about the amplitude and phase angle of the positive- and negative-sequence components of the grid voltage vector.

Finally, the PI controller of the DDSRF PLL works on the decoupled *q*-axis signal of the positive-sequence SRF (v^{*}) and performs the same function as in an SRF PLL, aligning the positive-sequence voltage with the *d*-axis. This signal is free of ac components due to the effect of the decoupling networks; the bandwidth of the loop controller can be consequently increased.

B. DSOGI PLL

The operating principle of the DSOGI PLL for estimating the positive- and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the $\alpha\beta$ stationary reference frame, as explained in [35]. The diagram of the DSOGI PLL is shown in Fig. 4. As it can be noticed, the ISC method is implemented by the positive-sequence calculation block.

To apply the ISC method, it is necessary to have a set of signals, $v\alpha$–$v\beta$, representing the input voltage vector on the $\alpha\beta$ stationary reference frame together with another set of signals, $qv\alpha$–$qv\beta$, which are in quadrature and lagged with respect to $v\alpha$–$v\beta$. In the DSOGI PLL, the signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI), which is an adaptive band pass filter based on the generalized integrator concept [42]. At its output, the DSOGI provides four signals, namely, v'_{α} and v'_{β}, which are filtered versions of $v\alpha$ and $v\beta$, respectively, and qv'_{α} and qv'_{β}, which are the in-quadrature versions of v'_{α} and v'_{β}.

A conventional SRF PLL is applied on the estimated positive-sequence voltage vector, $v^{+}_{\alpha\beta}$ to make this synchro- nization system frequency adaptive. In particular, the v^{+}_{q} voltage vector is translated to the rotating SRF, and the signal on the *q*-axis, v^{+}_{q}, is applied at the input of the loop controller. As a consequence, the fundamental grid frequency (ω') and the phase angle of the positive-sequence voltage vector ($\theta^{+'}$) are estimated by this loop. The estimated frequency for the fundamental grid component is fed back to adapt the center frequency ω' of the DSOGI.

C. 3phEPLL

The enhanced phase-locked loop (EPLL) is a synchroniza- tion system that has proven to provide good results in single- phase synchronization systems [43]. An EPLL is essentially an adaptive bandpass filter, which is able to adjust the cutoff frequency as a function of the input signal. Its structure was later adapted for the three-phase case [44], in order to detect the positive-sequence vector of three-phase signals, obtaining the 3phEPLL that is represented in Fig. 5.

In this case, each phase voltage is processed independently by an EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency and jv_n', the second one being 90° with respect to v_n'. The resulting signals constitute the input for the computational unit. Owing to these in-quadrature signals, the instantaneous positive-sequence voltage component V+abc can be estimated by means of using the ISC method.

3. Discrete Implementation

The performance of the different structures under test is really dependent on their final digital implementation, particularly on the discretization approach made to their continuous equations [45]. This implementation is critical and should be studied in detail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL. Some methods, such as the forward Euler, the backward Euler, and the Tustin (trapezoidal) numerical integration, offer a good performance when used for discretizing other synchronization systems, as shown in [46] and [47]. However, Euler methods can be inadequate under certain conditions, due to the need of introducing additional sample delays [48]. Therefore, according to the specific needs of the presented topologies, this section will describe the discrete representation of each PLL individually. In order to facilitate the comprehension of the process, the different building blocks that appear at Figs. 3–5 will be referenced. The values of the different parameters used in each case are summarized in the Appendix.

A. DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained since the continuous representation of several parts does not change in the discrete domain. This is the case for the transformation blocks $T\alpha\beta$, $T_{dq}{+}1$, and $T_{dq}{-}1$, whose description can be found in general scope literature [49].

1) Positive- and Negative-Sequence Decoupling Networks: The decoupling network constitutes one of the most impor- tant contributions of this synchronization method. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain [41]. It is just necessary to consider one sample delay of θ', $\bar{v}_d{-}1$, $\bar{v}_q{-}1$, $\bar{v}_d{+}1$, and $\bar{v}_q{+}1$ in order to avoid algebraic loops.

Phase and Magnitude Estimator Discretization: In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 6). However, this does not affect the discretization of the phase and magnitude estimator since $v*d{+}1$ and $v*a{+}1$ act as the input of this block

$$\begin{bmatrix} v^*_{d^+1}[n+1] \\ v^*_{q^+1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^+1}[n+1] \\ v_{q^+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^-1}[n] \\ \bar{v}_{q^-1}[n] \end{bmatrix} \times \begin{bmatrix} v^*_{d^-1}[n+1] \\ v^*_{q^-1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^-1}[n+1] \\ v_{q^-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^+1}[n] \\ \bar{v}_{q^+1}[n] \end{bmatrix}. \quad (1)$$

The discrete controller and the integrator can be built using a backward numerical approximation. The frequency and phase can then be represented in the z-domain (2), considering $v^*_{q^+1}$ as the error to be minimized. In this equation, a feedforward of the nominal frequency is given by means of ωff

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q^{+1}}(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q+1}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \quad (3)$$

In these equations, a frequency feedforward has been intro- duced as an initial condition to ω'.

3) LPF Block Discretization: The amplitudes of the *dq* positive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse response (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency ωf , equal to half of the grid frequency, was originally proposed in [41]; hence, the same transfer function has been implemented in this paper for evaluation purposes in

$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$
$$x[n+1] = y[n]. \quad (4)$$

B. DSOGI-PLL Discretization

1) DSOGI-QSG Block Discretization: As was previously mentioned in Section II, the DSOGI-based quadrature sig- nal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). Therefore, each SOGI-based quadrature signal generator can be discretized individually, thus facilitating its mathematical description. In Fig. 7, the block diagram of the implemented SOGI is shown.

This quadrature signal generator (QSG) is a linear system itself; therefore, a discrete representation can be systematically obtained if the continuous state space is previously deducted. The equations of the SOGI state space appear detailed in (5). where *v* constitutes the input while v' and qv' are the two in- quadrature output signals

$$\left.\begin{aligned} \dot{x}_n &= A \cdot x_n + B \cdot v \\ y_n &= C \cdot x_n \end{aligned}\right\}; \quad x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \; y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix}$$
$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k \cdot \omega' \end{bmatrix} \; B = \begin{bmatrix} 0 \\ k \cdot \omega' \end{bmatrix} \; C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix}. \quad (5)$$

The discretization of this system has been performed using trapezoidal integrators, as they offer a better detection of the phase, which is important when dealing with sinusoidal signals [22]. The symbolic values of each matrix of (7) are detailed in (6), shown at the bottom of the page. In these matrices, *Ts* is the sampling time of the discrete system, $\omega\_[n]$ is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and *k* is the SOGI gain [14]

$$x[n+1] = A' \cdot x[n] + B' \cdot v[n]$$
$$y[n] = C' \cdot x[n] + D' \cdot v[n]. \qquad (7)$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure presented in (8) [50], [51]

$$A' = \left(I + \frac{A \cdot T_s}{2}\right)\left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$B' = \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot B$$
$$C' = T_s \cdot C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$D' = C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot \frac{B \cdot T_s}{2}$$
$$A' = \gamma \begin{bmatrix} 4 + 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 & 4T_s \\ -4T_s \cdot \omega'[n]^2 & 4 - 2T_s \cdot k \cdot \omega'[n] - T_s^2 \cdot \omega'[n]^2 \end{bmatrix},\ B' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ 4k \cdot \omega'[n] \end{bmatrix}$$
$$C' = \gamma \begin{bmatrix} -2T_s^2 \cdot \omega'[n]^2 & 4T_s \\ 2T_s \cdot \omega'[n] \cdot (2 + T_s \cdot k \cdot \omega'[n]) & 2T_s^2 \cdot \omega'[n] \end{bmatrix},\ D' = \gamma \begin{bmatrix} 2T_s \cdot k \cdot \omega'[n] \\ k \cdot T_s^2 \cdot \omega'[n]^2 \end{bmatrix}$$
$$\gamma = \frac{1}{4 + 2 \cdot T_s \cdot k \cdot \omega'[n] + T_s^2 \cdot \omega'[n]^2} \qquad (6)$$

where T_S is the sampling time.
The resulting discrete system is the best option as it reduces the need of using additional delays for breaking algebraic loops that appear using other methods which do not consider the SOGI QSG as a whole.

2) SRF PLL Discretization: The frequency and phase detection is obtained by means of the SRF PLL shown in Fig. 8. The discretization of the controller and the integrator is performed using the backward numerical approximation.
The frequency and phase can then be represented in the z-domain, as shown in (9), where *v+ q* constitutes the error to be minimized

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z - 1} \cdot V^*_{q^{+1}}(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z - 1} \cdot W'(z). \qquad (9)$$

It can be noticed that the previous equations in (9) are equal
to (2), as, in both cases, an SRF PLL is implemented. Like- wise, the sample-based representation of (9) can be written as shown in

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q^{+1}}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q^{+1}}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \qquad (10)$$

C. 3phEPLL Discretization

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phase voltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

1. QSG Block—EPLL Discretization: The block diagram of the EPLL implemented in this paper is presented in Fig. 9

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$\begin{aligned}\dot{A}'(t) &= k \cdot e(t) \cdot \cos\theta'(t)\\ \dot{\omega}'(t) &= -k_i \cdot e(t) \cdot \sin\theta'(t)\\ \dot{\theta}(t) &= \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t).\end{aligned} \tag{11}$$

The discrete state space variable representation was de- scribed in [44] using a forward Euler approximation to reach satisfactory results; therefore, the same method has been im- plemented here

$$\begin{aligned}&e[n+1] = u[n+1] - v'[n]\\ &A'[n+1] = A'[n] + T_S \cdot k \cdot e[n] \cdot \cos(\theta'[n])\\ &\omega'[n+1] = \omega'[n] - T_S \cdot k_I \cdot e[n] \cdot \sin(\theta'[n])\\ &\theta'[n+1] = \theta'[n] + T_S \cdot \omega'[n] - T_S \cdot k_P \cdot e[n] \cdot \sin(\theta'[n]).\end{aligned} \tag{12}$$

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadrature signals

$$\begin{aligned}&v'[n+1] = A'[n+1] \cdot \cos(\theta'[n+1])\\ &qv'[n+1] = -A'[n+1] \cdot \sin(\theta'[n+1]).\end{aligned} \tag{13}$$

This type of discretization method needs a more accurate tuning, due to the fact that the stable regions of the s-plane and z-plane are different [52]. However, its major simplicity, compared to the Tustin or backward integration, benefits from the computational speed of this block.

1) Computational Block Unit: The description for this block is the same in both discrete and continuous domains. Neverthe- less, specific equations are used in this paper, as shown in (14).

2) Phase and Magnitude Detection Block: This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the positive-sequence fundamental component. Its discretization is equal to that shown in (12)

$$\begin{aligned}v_a^+[n] &= \frac{1}{3}v'_a[n] - \frac{1}{6}\left(v'_b[n] + v'_c[n]\right) + \frac{1}{2\sqrt{3}}\left(jv'[n]_b - jv'_c[n]\right)\\ v_c^+[n] &= \frac{1}{3}v'[n]_c - \frac{1}{6}\left(v'_a[n] - v'_b[n]\right) + \frac{1}{2\sqrt{3}}\left(jv'_a[n] - jv'_b[n]\right)\\ v_b^+[n] &= -\left(v_a^+[n] + v_c^+[n]\right).\end{aligned} \tag{14}$$

However, for the phase and magnitude detection block, the outputs are the positive sequence magnitude and phase, which correspond directly with the states $\theta\_$ and $A\_$, respectively.

4. Testing signals and experimental setup

Following the representations in the discrete domain already deducted, the different PLL algorithms have been implemented in a control board based on a floating-point Texas Instruments TMS320F28335 DSP at 150 MHz (6.67-ns cycle time). Their capability to perform a fast and accurate synchronization has been tested in the laboratory under different grid fault scenarios, where the three-phase voltage waveforms experience transients due to the appearance of voltage sags, frequency variations, and harmonic pollution. These unbalanced and distorted input voltages were generated by means of an ac programmable source and an auxiliary transformer. The layout of the experimental workbench used in this paper is presented in Fig. 10. Six representative faulty and distorted scenarios have been selected for evaluating the three synchronization systems under test.

• *Voltage sags*: In Table I, the characteristics of four selected voltage sags have been summarized. It is worth to mention that these sags are the most characteristic ones that affect wind power systems. In Table I, the magnitude and the phase of the symmetrical components of the voltage dur- ing the fault period are indicated in each case, assuming that the prefault voltage is always equal to $V^+ = 100$, $V^- = 0$, and $V^0 = 0$.

As can be seen in the table, three of the proposed sags give rise to unbalanced voltages, as explained in [37] and [38], and, hence, to positive- and negative-sequence components. The presence of the negative sequence during the fault allows a more rigorous analysis of the synchronization capability of the different algorithms under test. Moreover, unbalanced faults constitute 95% of the voltage sags that affect distributed generation systems.

In order to obtain the aforementioned dips, different faults have been emulated with the programmable ac source at the primary winding of the transformer, as indicated in Fig. 11. De- pending on the fault topology as well as on the connection of the transformer, the desired voltage waveforms at the measurement point, indicated in Table I, are finally obtained, acquired, and later processed by the DSP.

• *Harmonic-polluted voltage (8% THD)*: According to the EN50160 standard [53], the THD of the voltage wave- forms at the output of a generation facility cannot be higher than 8%. Considering this requirement, Table II shows the harmonic composition used for evaluating the performance of the grid synchronization systems under test when the grid voltages become distorted.

• *Grid voltage frequency jumps*: By means of the pro- grammable source, a 10-Hz jump (from 50 to 60 Hz) in the frequency value of the positive sequence has been applied to analyze the response of the frequency adaptive structures under test.

In the following section, the responses of the DDSRF PLL, DSOGI PLL, and 3PhEPLL under these transient conditions will be compared.

5. Experimental Performance of the PLLs under test

A. Behavior in Case of Voltage Sags

1) Type "A" Sag Test: This kind of voltage sag appears as a consequence of three-phase faults that give rise to high short circuit currents and, hence, to a balanced voltage drop in the network. As Fig. 12(e) and (i) shows, the DDSRF PLL and the DSOGI PLL produce a good response, as both systems achieve a very fast detection (20 ms) of the positive-sequence compo- nents (less than two cycles). The response of the 3phEPLL, depicted in Fig. 12(m), also shows a good response, but with a larger transient in the positive-sequence estimation.

2). Type "B" Sag Test: This kind of fault permits analyzing the behavior of the PLLs under test in the presence of zero- sequence components at the input. The Clarke transformation used in DSOGI PLL and DDSRF PLL to extract the $\alpha\beta$ com- ponents enhances the response of this synchronization system when the faulty grid voltage presents zero-sequence compo- nents. Their responses, as shown in Fig. 12(f) and (j), are fast and accurate. On the other hand, the 3phEPLL does not cancel out the zero-sequence component from the input voltage, some- thing which may affect the dynamics of the positive-sequence estimation loop. However, this effect is further attenuated by the computational unit, as Fig. 12(n) shows; the steady-state response is also reached with no great delay, as detailed in Fig. 12(n), showing the good behavior of this PLL under these conditions.

3).Type "C" and "D" Sag Tests: These kinds of sags appear due to phase-to-ground and phase-to-phase short circuits at the primary winding of the transformer, respectively, as shown in Table I. In a distribution network, these distortions are more common than the previous ones, as they are the typical grid faults caused by lightning storms. As depicted in Fig. 12(g)–(p), all three PLLs permit detecting the positive sequence between 20 and 30 ms; however, the 3phEPLL has a slower stabilization, as shown in Fig. 12(o) and (p). This effect is a bit more noticeable with the "C" sag, where the combination of the phase jump and the magnitude change of two phases occurs, as shown in Fig. 12(o).

B. Frequency Changes (50–60 Hz)

In this experiment, similar results are obtained with the DDSRF and the DSOGI PLL, as can be seen in Fig. 13(a)–(d). The low overshooting in the amplitude estimation in both cases [see Fig. 13(a) and (c)] assists the good phase and frequency detection, as shown in Fig. 13(b) and (d). Likewise, the response of the 3phEPLL shows a similar settling time, as shown in Fig. 13(e); however, the initial oscillation in the amplitude estimation of the voltage contributes to slightly de- lay the stabilization of the frequency magnitude, as displayed in Fig. 13(f).

C. Polluted Grids (*THD* = 8%)

The 3phEPLL behaves as a bandpass filter for the input signal, something that permits filtering the input without adding extra filters. As can be seen in Fig. 14(d), the 3phEPLL offers the best filtering capability among the PLLs under test, with a clear and undistorted estimation of the magnitude and phase of the input.

The response of the DDSRF PLL, depicted in Fig. 14(b), which has a first-order filter at the output, is even

better than the one provided by the DSOGI PLL, due to the latter's low- pass filtering behavior. Although the DSOGI PLL also behaves as well as a bandpass filter, the tuning of its parameters, which permits a faster stabilization of the estimated signal in the previous tests, plays against its immunity in front of harmonics, as shown in Fig. 14(c), giving rise to small oscillations in the positive-sequence estimation.

6. Evaluation of the Computational Burden Time

The computational cost in the floating-point TMS320F28335 DSP, which is considered as a microcontroller by the brand itself, has been evaluated for each case. However, an initial qualitative analysis can be done if each algorithm is divided into its fundamental operations. The different types of ba- sic operations, as well as how many times they were used in each algorithm, are summarized in Table III, where the shadowed cells indicate which PLL is used the least often by each operator.

The results from Table III seem to indicate that the DDSRF PLL and the DSOGI PLL could be the fastest algorithms. On the other hand, the number of trigonometrical functions that the 3phEPLL has to perform plays against its computational cost. This statement can be subsequently confirmed with the exper- imental burden time measured for each PLL when processing one cycle, as shown in Table IV.

Regarding the results of Table IV, the DDSRF PLL performs the fastest loop. In spite of the high number of additions and multiplications to be calculated, the DSOGI PLL holds second position in this burden-time comparative, although the differences with respect to the DDSRF are not quite significant. Finally, it can be observed that the greatest burden time is obtained with the 3phEPLL.

IV. FIGURES & TABLES

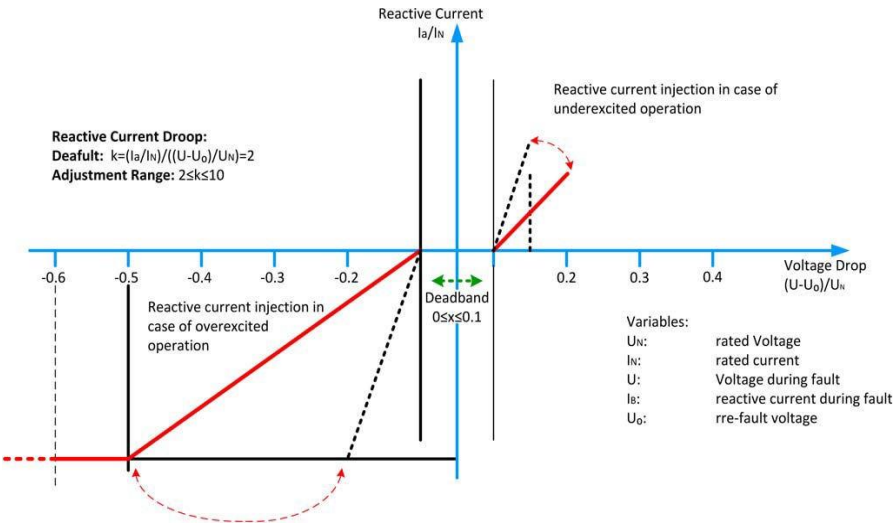


Fig. 1. E-on voltage support requirement in the event of grid fault.

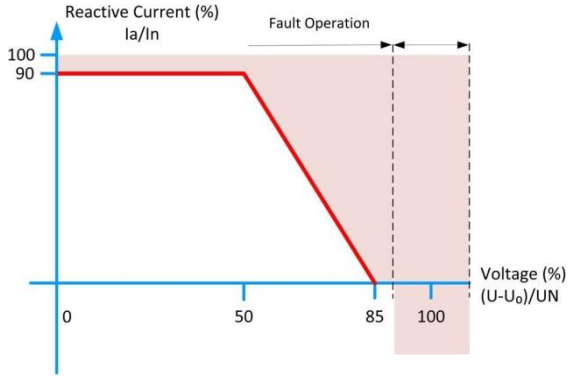


Fig. 2. REE voltage support requirement in the event of grid fault.

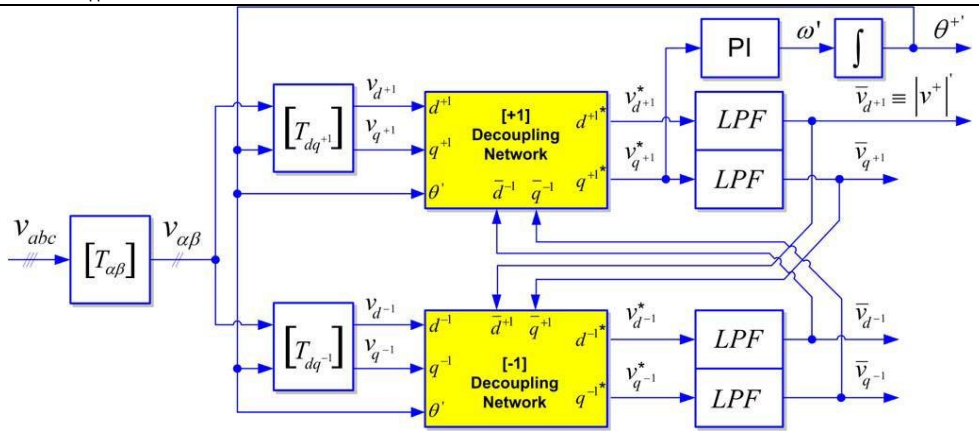


Fig. 3. DDSRF-PLL block diagram.

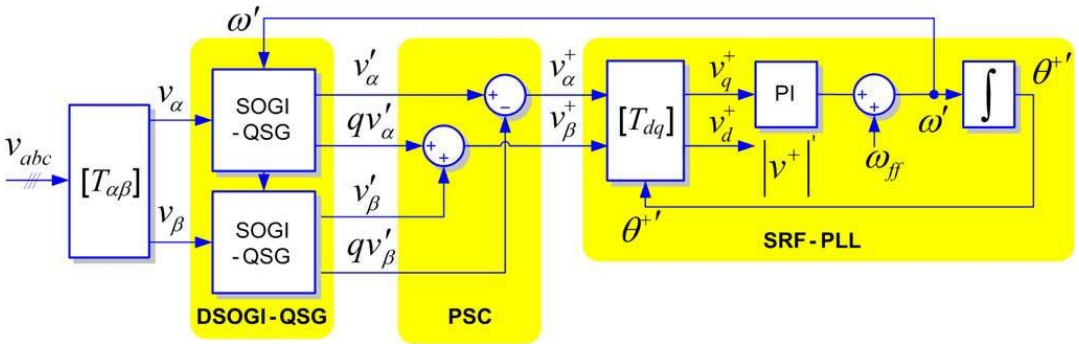


Fig. 4. DSOGI-PLL block diagram.

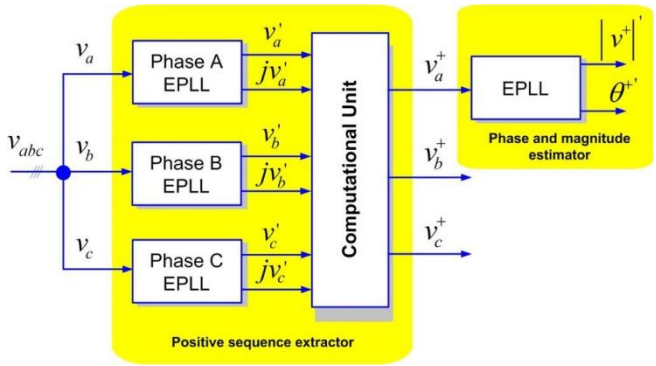


Fig. 5. 3phEPLL block diagram.

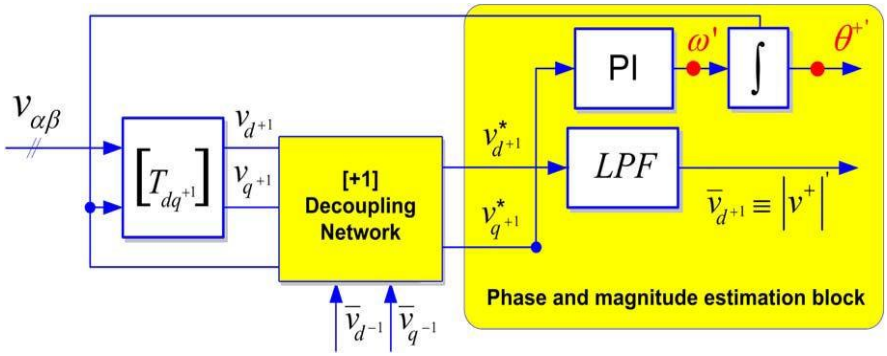
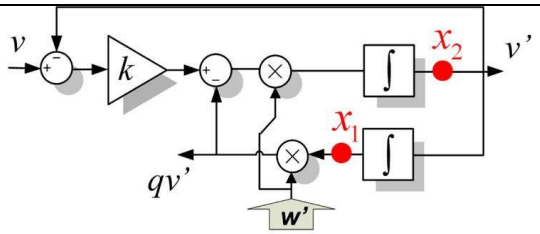


Fig. 6. Phase and magnitude estimation loop of the DDSRF PLL.



SOGI - QSG

Fig. 7. Quadrature signal generator based on a second order generalized integrator (SOGI QSG).

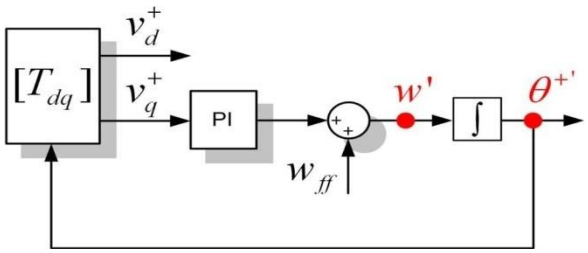


Fig. 8. State variables of the SRF-PLL block.

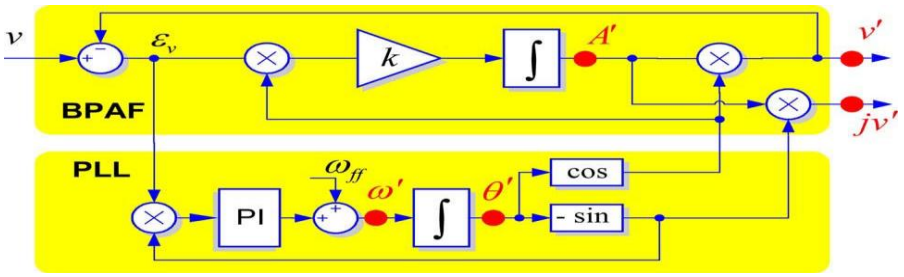


Fig. 9. Quadrature signal generator based on an EPLL structure.

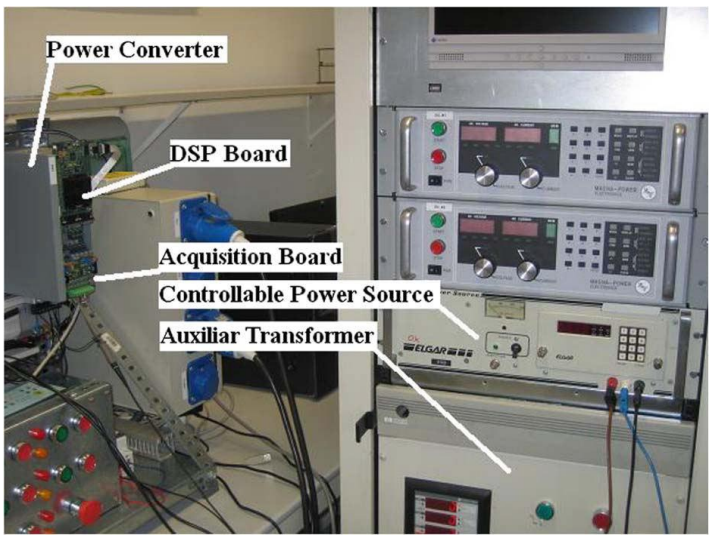


Fig. 10. Experimental setup for testing three different synchronization algorithms

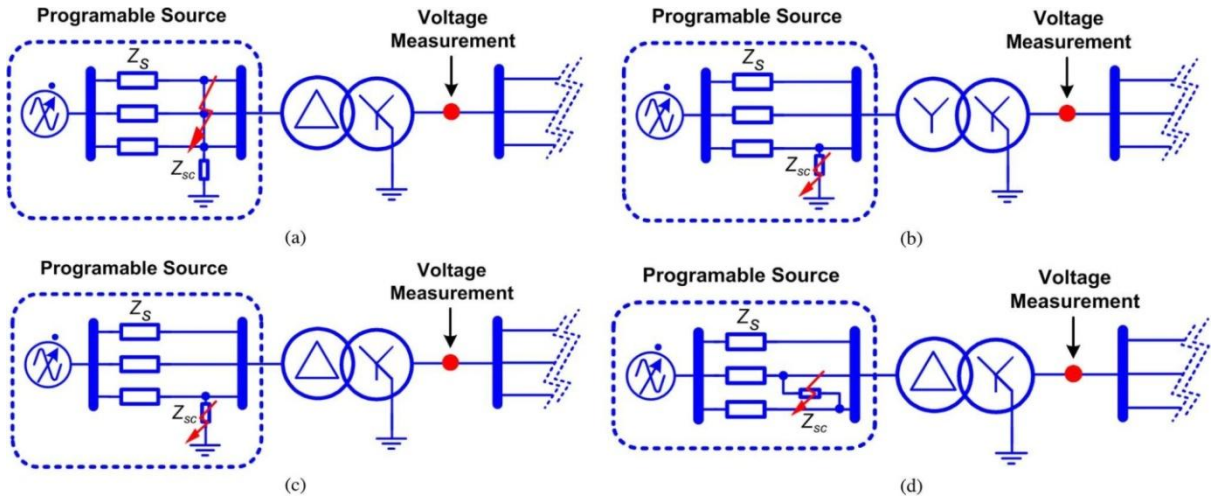


Fig. 11. Generation of grid voltage sags in the experimental setup. (a) Generation of a Type "A" voltage sag. (b) Generation of a Type "B" voltage sag. Generation of a Type "C" voltage sag. (d) Generation of a Type "D" voltage sag

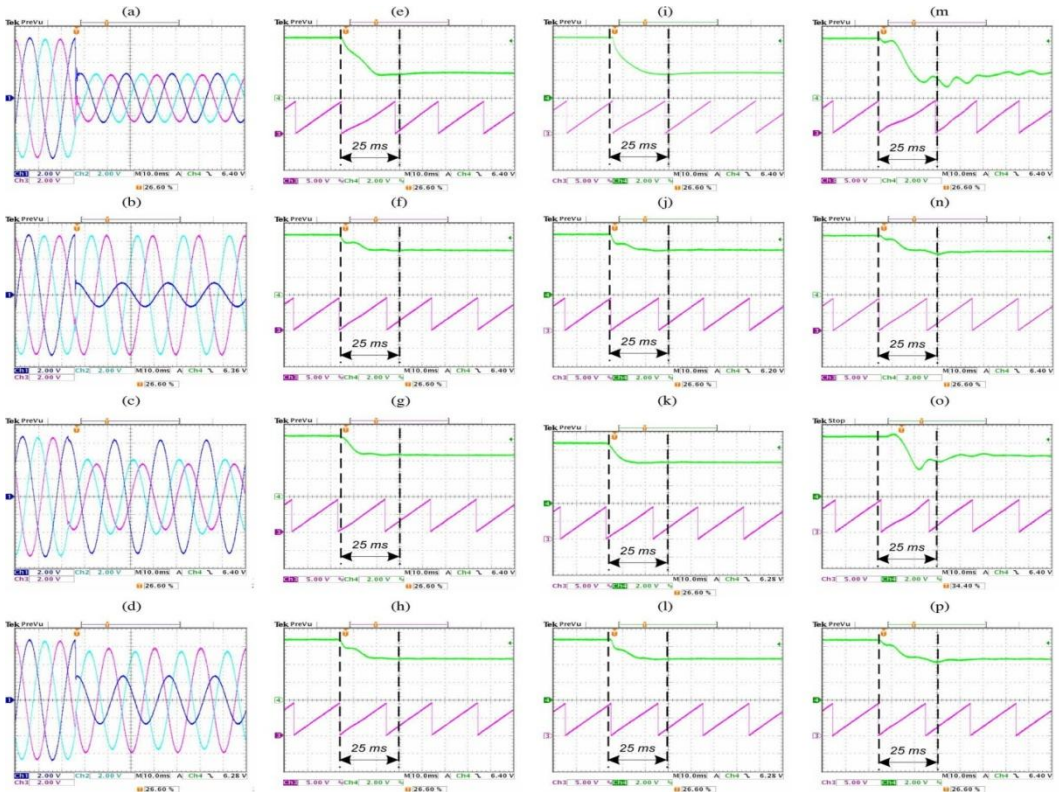


Fig. 12. Amplitude and phase estimation of the three tested PLLs in case of four types of sag. (a)–(d) Input signal (V). (e)–(h) Amplitude (V) and phase (rad) detection for the DSRF PLL. (i)–(l) Amplitude (V) and phase (rad) detection for the DSOGI PL. (m)–(o) Amplitude (V) and phase (rad) detection for the 3phEPLL. Scaling factors: Amplitude = 1 : 150; phase = 1 : 7.

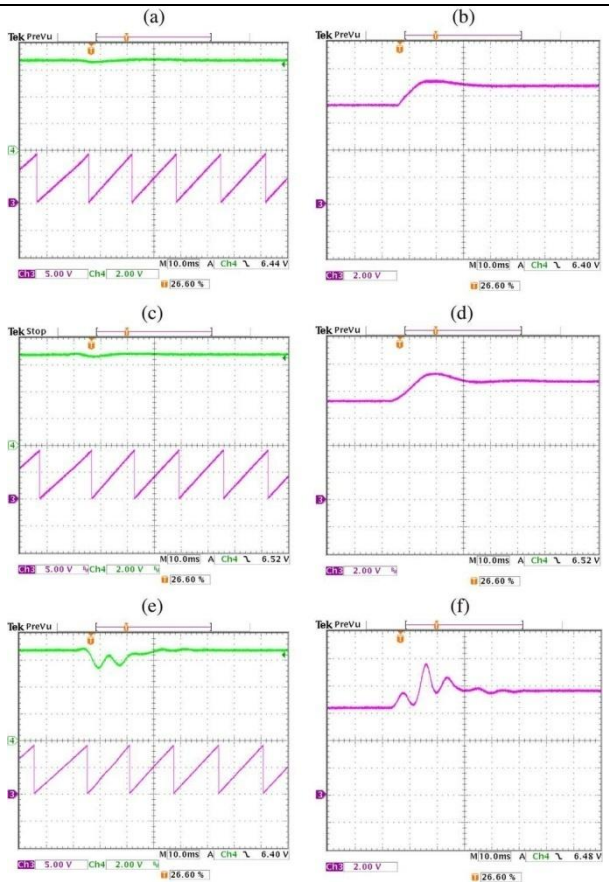


Fig. 13. Amplitude, phase, and frequency estimation of the three tested PLLs in a frequency jump. (a) and (b) Amplitude (V), phase (rad), and frequency detection for the DDSRF PLL. (c) and (d) Amplitude (V), phase (rad), and frequency detection for the DSOGI PLL. (e) and (f) Amplitude (V), phase (rad), and frequency detection for the 3phEPLL. Scaling factors: Amplitude = 1 : 150, phase = 1 : 7, and frequency 1 : 70.

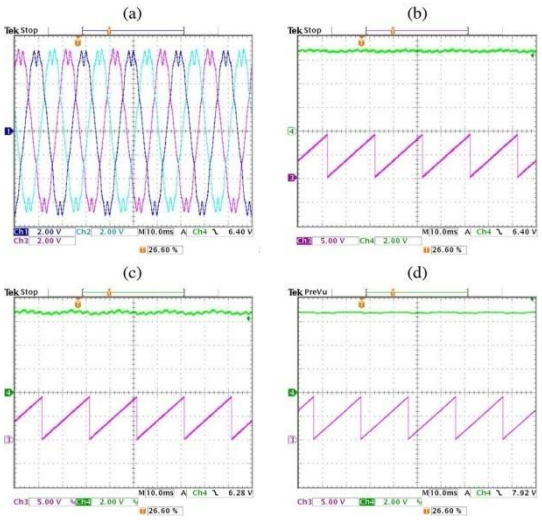
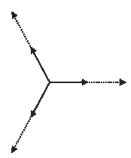
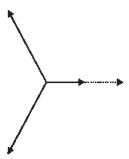
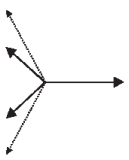
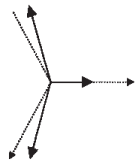


Fig. 14. Amplitude and phase estimation of the three tested PLLs in a polluted grid (THD = 8%). (a) Input signal (V). (b) Amplitude (V) and phase detection (rad) for the DDSRF PLL. (c) Amplitude (V) and phase detection (rad) for the DSOGI PLL. (c) Amplitude (V) and phase detection (rad) for the 3phEPLL. Scaling factors: Amplitude = 1 : 150; phase = 1 : 7.

Table I Properties of the testing voltage sags

A Sag	B Sag	C Sag	D Sag
$\begin{cases} V^+ = 40\angle -40^\circ \\ V^- = 0\angle 0^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$	$\begin{cases} V^+ = 73.\hat{3}\angle -10^\circ \\ V^- = 26.\hat{6}\angle 170^\circ \\ V^0 = 26.\hat{6}\angle 170^\circ \end{cases}$	$\begin{cases} V^+ = 67.37\angle -5.7^\circ \\ V^- = 27.81\angle 2.2^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$	$\begin{cases} V^+ = 67.37\angle -5.7^\circ \\ V^- = 27.81\angle -177.8^\circ \\ V^0 = 0\angle 0^\circ \end{cases}$
			

Positive, negative and homopolar sequence vectors during the fault conditions for the different sags

Table II Harmonic composition for the test

Order of the harmonic	*THD (%)*
2^{nd}	2%
4^{th}	1%
5^{th}	5%
7^{th}	4%
11^{th}	3%
13^{th}	3%

Values of individual harmonic voltages at the supply terminals for orders up to 25, given in percent of the nominal supply voltage in RMS

Table III Number of operations performed by each PLL

Structure	A	M	T	S	D
DDSRF-PLL	22	32	12	14	0
DSOGI-PLL	38	86	4	8	2
3phEPLL-PLL	42	41	19	16	0

A = Addition M = Multiplication T = Trigonometric S = Variable storage D = Division. Type and number of operations in each PLL. The shadowed cells indicate the synchronization system that is used the least number of times by each operator.

Table IV Computational cost evaluation

Structure	Execution Time
DDSRF-PLL	$5.41\mu s$
DSOGI-PLL	$5.91\mu s$
3phEPLL-PLL	$8.36\mu s$

Global burden time of one cycle of instructions for each PLL programmed in a TMS320F28335 DSP.

Table V Tuning parameters of the analyzed PLLs

DDSRF-PLL	**Values**
T_s	$100\mu s$
k_p	2.22
k_i	246.74
ω_{ff}	314.1592 rad/s
ω_f	157.0796 rad/s
DSOGI-PLL	**Values**
T_s	$100\mu s$
k_p	2.22
k_i	61.7
k	$\sqrt{2}$
ω_{ff}	314.1592 rad/s
3phEPLL-PLL	**Values**
T_s	$100\mu s$
k_p	5
k_i	450
k_v	500
ω_{ff}	314.1592 rad/s

V. CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions.

The DDSRF PLL and the DSOGI PLL allow estimating the ISCs of a three-phase system working in the $\alpha\beta$ reference frame, while the 3phEPLL uses the "*abc*" reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as com- pared to the 3phEPLL, without affecting its performance.

The synchronization capability of the three PLLs under test has been shown to be fast and accurate under faulty scenarios, allowing the detection of the positive sequence of the voltage in 20–25 ms in all cases; however, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response.

The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater bandpass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent bandpass filtering structure, its response is

more affected by harmonics.

Although all three have been shown to be appropriate for synchronizing with the network voltage in distributed power generation applications, mainly PV and wind power, the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better tradeoff between the presented systems, making them particularly suitable for wind power applications.

VI. APPENDIX

The parameters used for tuning the different advanced syn- chronization systems analyzed in this paper are summarized in Table V.

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