International Journal of Latest Engineering and Management Research (IJLEMR)
ISSN: 2455-4847
www.ijlemr.com || REETA-2K16 ǁ PP. 536-543

Voltage Unbalance and Harmonics Compensation for Islanded Microgrid Inverters

K.BHANU TEJA[1]
J T RAMALINGESWAR[2]
[1](M.Tech Scholar,Dept of EEE , Sri Venkateswara Engineering College for Women, Karakambadi, Tirupati, AP, India)
[2](Assistant Professor, Dept of EEE, Sri Venkateswara Engineering College for Women, Karakambadi, Tirupati, AP, India)

ABSTRACT : Voltage source inverters (VSIs) are usually used for all kinds of distributed generation interfaces in a microgrid. It's the microgrid's superiority to power the local loads continuously when the utility fails. When in islanded mode the voltage and frequency of the microgrid are determined by the VSIs, therefore the power quality can be deteriorated under unbalanced and nonlinear loads. A voltage unbalance and harmonics compensation strategy for the VSIs in islanded microgrid is proposed in this paper.. In this paper, a control strategy with low bandwidth communications for paralleled three-phase inverters is proposed to achieve satisfactory voltage unbalance compensation. The proposed control algorithm mainly consists of voltage/current inner loop controllers, a droop controller, a selective virtual impedance loop, and an unbalance compensator. The inner loop controllers are based on the stationary reference frame to better mitigate the voltage distortion under nonlinear loads. Droop control and selective virtual impedance loop achieve accurate current-sharing when supplying both linear and non- linear loads. Moreover, by adjusting voltage references according to the amplitude of the negative sequence voltage, the unbalance factor, which is mainly caused by single phase generators/loads, can be mitigated to an extremely low value. Finally, an AC microgrid which includes three three-phase three-leg inverters was tested in order to validate the proposed control strategy.

KEYWORDS : Controllers, droop control, Microgrids, virtual impedance, voltage unbalance compensation

1.INTRODUCTION

The introduction of the paper should explain the nature of the problem, previous work, purpose, and the contribution of the paper. The contents of each section may be provided to understand easily about the paper. In recent years, dispersed energy resources (DERs), such as wind turbines, photovoltaic systems and micro-turbines, have gain a great increasing interest since they are economic and environment friendly. In general, power electronic converters are used as interfaces between DERs and the grid [1], suchthat electrical power with good quality and high reliability can be delivered to the load or utility grid, as shown in Fig. 1. This paper focuses on islanded microgrids where the interfacing converters mainly operate as voltage sources to participate on the voltage and frequency regulation while sharing at the same time active and reactive power accurately by adjusting output voltage phase angles and amplitudes. However, it is also preferred that those converters could provide power quality management ability, in such a way that we can take full use of the converters available capacity. It is well known that power quality issues, especially voltage/current unbalances and voltage/current distortions have become more and more serious in modern power system. For instance, in islanded microgrids

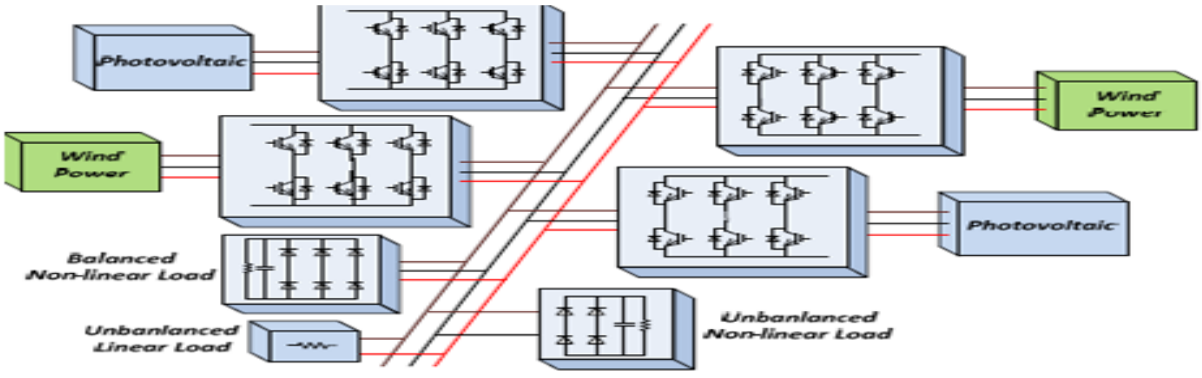

Fig. 1. General architecture of a microgrid.

the voltage unbalance problem is a salient issue mainly produced by the use of single-phase generators/loads and it can lead to instability and power quality issues. In order to enhance the voltage waveform quality, several components to deal with the voltage unbalance compensation have been developed, such as static var compensator (STATCOM) [2], series active power filter [3] and shunt active power filter[4] However, all these compensation methods utilize additional power converters to inject negative sequence reactive power. Only a few works compensate the unbalanced voltage by utilizing the DG interfacing converters. In [5], the DG inverter is controlled to inject negative sequence current to balance the common bus voltage. However, a surplus converter capacity is needed to generate the negative sequence current and the injecting current might be too high under severe unbalance conditions. In the previous work [6], an unbalance compensation method is proposed by sending proper control signals to DGs local controllers. However, the negative sequence component of the common bus voltage is hard to suppress, since the microgrid central controller (MGCC) uses the voltage unbalance factor as a main control variable, which value is reduced by the positive sequence voltage.

In order to overcome these drawbacks, this paper proposes a control scheme located in the MGCC which directly acts over the negative sequence voltage. Section II initially elaborates on the control design of local controllers, mainly including inner voltage/current loops, virtual impedance loop and droop controller, and then the system modeling is introduced. Section III will investigate the strategy of the proposed direct voltage unbalance compensator. Experimental results of a three paralleled inverters system is analyzed and discussed in Section VI. Finally, conclusions are presented in Section V.

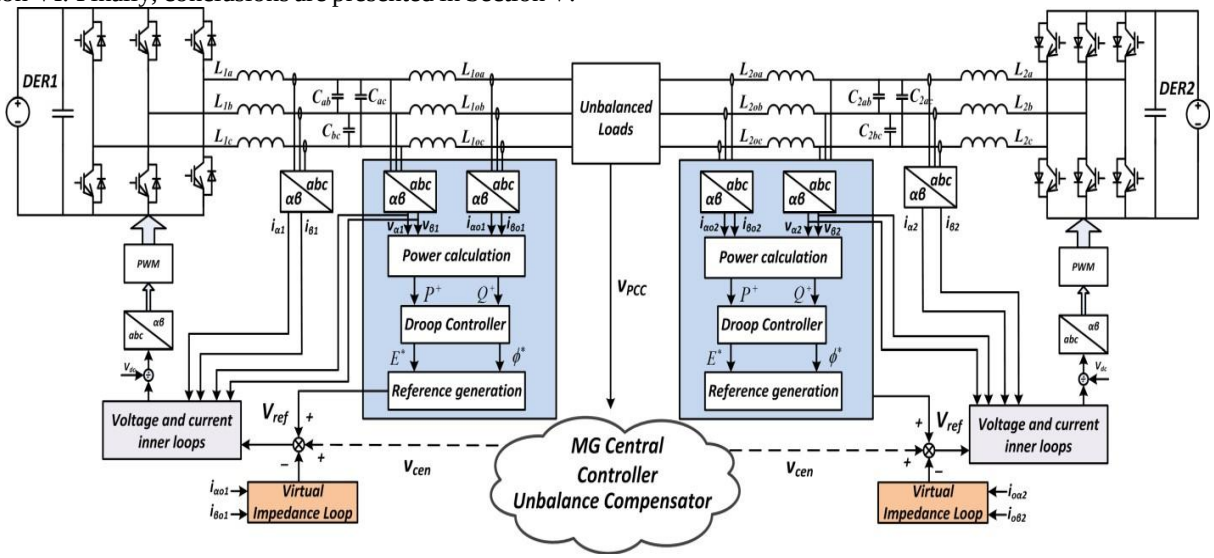

Fig. 2. Implementation of the local controllers.

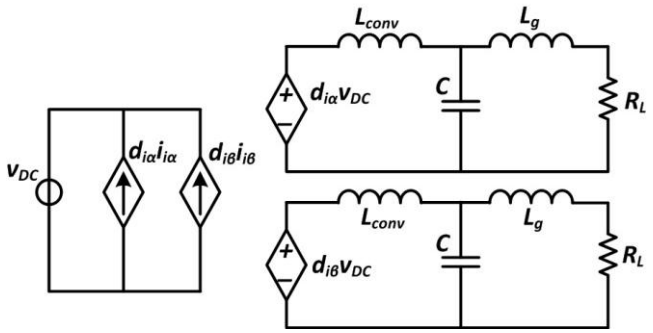

Fig. 3. Small signal model of single inverter.

2.LOCAL CONTROLLER DESIGN

Fig. 2 depicts the control strategy of inverter local controllers. LCL filter is adopted here, but it actually operates as a conventional LC filter with a coupling inductor. The main function of the grid side inductor is to optimize the dynamic performance and to shape the output impedance. Also its current is measured for power calculation and virtual impedance which will be explained later.

2.1 Inner Loop Design

It can be seen from Fig. 2 that the inner loops are implemented in two-phase stationary frame and all the measured voltage and current are transformed from *abc* to *αβ* coordinates, thus the computational burden is reduced significantly. Both voltage and current controllers are based on proportional+resonant (*PR*) controller instead of the conventional proportional+integrator (*PI*) controller. The reason is that *PR* controller can provide infinite gain at the selected resonant frequency to provide satisfactory tracking performance. In other words, the performance of *PR* controller at selected resonant frequency is conceptually similar to the performance of *PI* controller at 0Hz [7-9]. Also, in order to mitigate the voltage and current distortion under nonlinear loads, the *PR* controllers are tuned at fundamental frequency, 3^{rd}, 5^{th}, 7^{th}, 9^{th} and 11^{th} order harmonics.

Modeling of the main power circuit and the inner loop controller in synchronous reference frame is established here to obtain the close loop transfer function. By using *abc/αβ* transformation in the power plant and neglecting the zero quadrature components, the three phase inverter can be expressed as a decoupled two phase system. Fig.3 shows the small signal model of the decoupled two phase system. It is worthy noting that only one inverter is depicted here to simplify the figure.

According to the small signal model, the control scheme can be depicted in Fig. 4. The close loop transfer function is derived in (1):

$$v_c(s) = v_o^*(s) - Z_o(s) i_o(s) = \frac{G_v(s) G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} v_{ref}(s) - \frac{Ls + G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} i_o(s)$$

where $v_C(s)$ is the capacitor voltage, $v^*(s)$ is the open circuit voltage, $i_O(s)$ is the output current, $Z_O(s)$ is the equivalent output impedance, $v_{ref}(s)$ is the voltage reference, L is the converter side inductor, C is the filter capacitor. $G_V(s)$, $G_i(s)$ and $G_{PWM}(s)$ are the transfer function of voltage controller, current controller and *PWM* delay respectively. Their transfer function can be expressed as

$$G_v(s) = k_{vp} + \sum_{h=1,3,5,7,9,11} k_{hvr} \frac{s}{s^2 + (h\omega)^2} \quad (2)$$

$$G_i(s) = k_{ip} + \sum_{h=1,3,5,7,9,11} k_{hir} \frac{s}{s^2 + (h\omega)^2} \quad (3)$$

$$G_{PWM}(s) = \frac{1}{1 + 1.5T_s s} \quad (4)$$

ref :

where φ^* and E^* are the amplitude and phase angle of the output voltage reference while $E0$ and $\varphi 0$ are the amplitude and phase angle of the output voltage at no voltage at no load condition, P^+ and Q^+ are the instantaneous fundamental positive sequence active and reactive power, respectively, and and P^+ are Q^+ reference of fundamental positive sequence active and reactive power, respectively; m_P and m_I are the proportional and integral coefficients of active power controller, respectively. mI mainly influence the dynamic characteristic of the system since it adds inertia to the system; n_P is the integral coefficients of reactive power controller.

It can be seen from (7)-(10) that the higher the droop coefficients is, the better power sharing can be achieved. However, the voltage and frequency deviation will also become larger when the droop coefficients become bigger. This tradeoff can be

compensated by introducing secondary controller, as illustrated in [10]. Hence, both the proportional coefficients should be carefully selected according to (11) and (12): instantaneous reactive power theory [13], is followed by a low pass filter with a 2Hz cut-off

where Δf and ΔE are the maximum allowable deviation of frequency and amplitude from its nominal value, respectively.P and Q are the rated active and reactive power, respectively.

A positive-negative-sequence harmonic voltage/current component extractor [11-12] based on a second-order generalized integrator (*SOGI*) is implemented to assist the droop controller and the virtual impedance loop, which will be introduced in Section C. Since the fundamental positive sequence component extraction is almost the same with that of the fundamental negative sequence and harmonics, only the fundamental positive sequence voltage extractor is shown here in Fig. 7.

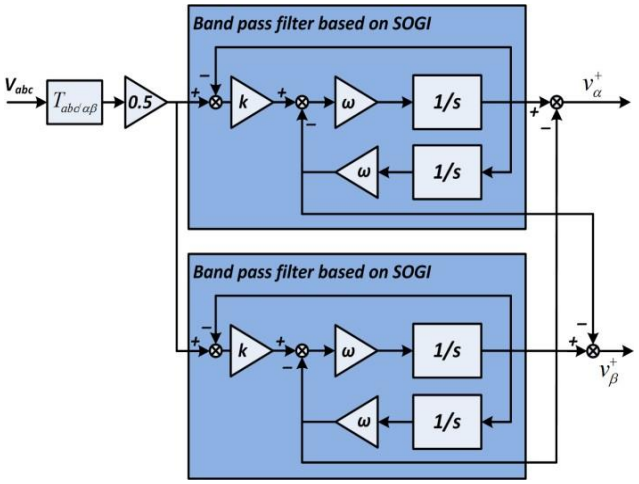

Fig. 7. Fundamental positive sequence component extractor.

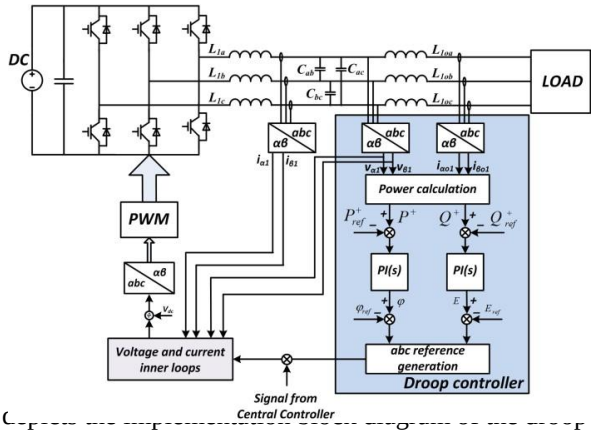

Fig. 8 [illegible] controller.

The power calculation block, based on the frequency, so that the power oscillation can be filtered out.

2.2 Virtual Impedance Loop

In order to share the power precisely between the distributed inverters, the output impedance of the inverter must be re-designed to mitigate the influence of control parameters and line impedance on the power sharing accuracy. Here, (1) can be rewritten as:

$$v_C(s) = G(s)\,v_{ref}(s) - \tilde{Z}_o(s)\,i_o(s) \quad (1)$$

where $G(s)$ represents the close loop transfer function of the inverter, and $Z_O(s)$ represents the close loop output impedance of the inverter. From the above equation, a two-terminal *Thevenin* equivalent circuit of the close loop inverter can be obtained, as shown in Fig. 9.

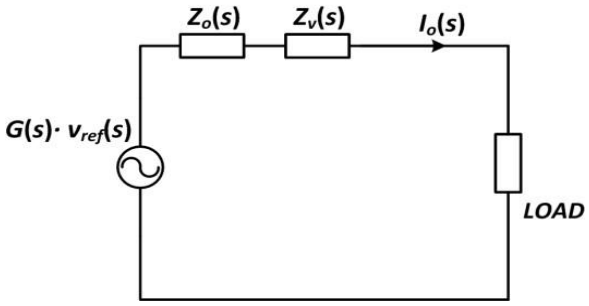

Fig. 9. Thevenin equivalent circuit of the close loop inverter.

If no control loop is implemented to compensate the output impedance, the amplitude of the output impedance at fundamental frequency and 3rd, 5th, 7th, 9th and 11th order harmonics is extremely small, as shown the blue curve in Fig.10. Thus, a virtual impedance loop must be added in the control block to fix the output impedance.

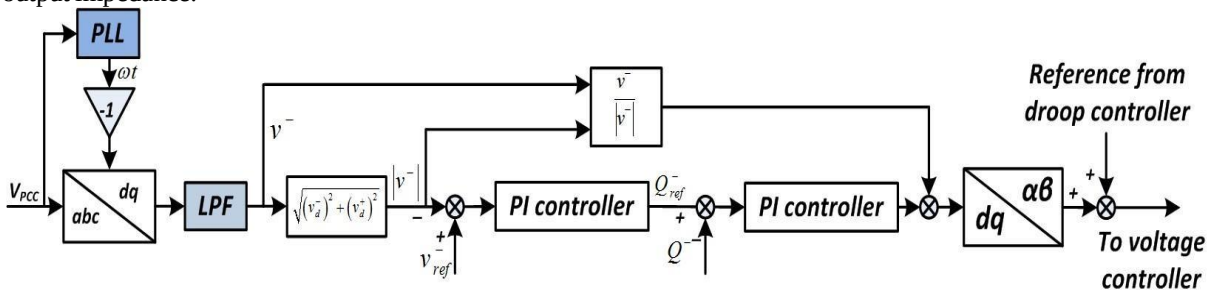

Fig. 12. Block diagram of the proposed unbalance compensator.

TABLE I.PARAMETERS OF POWERPLANTS

Parameters	*Symbol*	*Value*	*Unit*
Converter Side Inductors	L_{con}	*1.8*	*mH*
Grid Side Inductors	L_g	*1.8*	*mH*
Capacitors	*C*	*9*	*μF*
Nominal Voltage	*V*	*230*	*V*
Nominal Frequency	*f*	*50*	*Hz*
DC Voltage	*VDC*	*650*	*V*
Switching Frequency	f_s	*10*	*kHz*

TABLE II. CONTROL SYSTEMPARAMETERS

Voltage/Current Inner Loop Controllers		
Parameters	**symbol**	**value**
Voltage Loop Controller	k_{vp}, k_{vr}, k_{3vr} k_{5vr}, k_{7vr}, k_{9vr}, k_{11vr}	0.05,90,5,5,15,10,20
current loopcontroller	k_{ip}, k_{ir}, k_{3ir},k_{5ir}, k_{7ir}, k_{5ir}, k_{11vr}	*5, 200, 20, 10, 10, 10 10*

Primary Controller			
Parameters	**Symbol**	**Value**	**Unit**
Proportional Phase Droop	m_P	0.0005	Rad·s/W
Integral Phase Droop	m_I	0.00006	Rad/W

Proportional Phase Droop	n_P	0.002	V/Var
Virtual Resistor	R^+, R^-, R, R, R_7, R_9, R_{11}	1, 4, 4, 5, 5, 5, 5	Ω
Virtual Inductor	L_V	4	mH

Secondary controller

Parameters	Symbol	Value
Negative Sequence Voltage Reference	vref	0.5
Negative Sequence Voltage Controller	Kp_vneg, ki_vneg	5, 0.01
Negative Sequence Power Controller	Kp_Qneg, ki_Qneg	0.01, 0.5

3.EXPERIMENTAL RESULTS

In order to validate the correctness of the proposed control strategy, experiments have been carried out on a MG platform existing in the Microgrid Lab at Aalborg University [14]. The platform consists of three *Danfoss* three-phase DG inverters which share a common AC bus. In addition, the detailed electrical configuration is shown in Fig. 2 as well. An unbalanced resistive load is connected to the common AC bus to emulate unbalanced load conditions. The detailed power stage and control system specifications can be found in Table I and Table II.

Before t=2*s*, an unbalanced linear load is connected to the common AC bus and lead to the flowing of negative sequence current. Thus, voltage unbalance appears on the *PCC* voltage, as shown in Fig. 13(a). At the meantime, the output voltage of the three DGs has a good voltage quality, as illustrated in Fig. 16.

At t=2*s*, the direct unbalance compensation loop is enabled and then the corresponding compensation signal is sent to the DGs local controller. As expected, the unbalance factor significantly reduced from 5% to 0.2% after 10 seconds (as shown in Fig. 14). In addition, it can be seen from Fig. 13(b) and Fig. 16 that the decrease of the *PCC* voltage unbalance factor is achieved by means of deteriorates the DGs output voltage. To better illustrate the effect of the unbalance compensator, the negative sequence voltage at *PCC* is shown in Fig. 15. It is obvious that the PCC negative sequence voltage drops dramatically after the compensation enabled. Note that the unbalance factor (UF) is defined as (15):

$$UF = \frac{\sqrt{\left(v_d^-\right)^2 + \left(v_q^-\right)^2}}{\sqrt{\left(v_d^+\right)^2 + \left(v_q^+\right)^2}} \cdot 100 \qquad (15)$$

where v_d^+ and v_q^+ are the positive sequence of the PCC voltage respectively; v_d^- and v_q^- are the negative sequence of the *PCC* voltagerespectively

Fig. 13. *PCC* voltages: (a) Before compensation, (b) After compensation

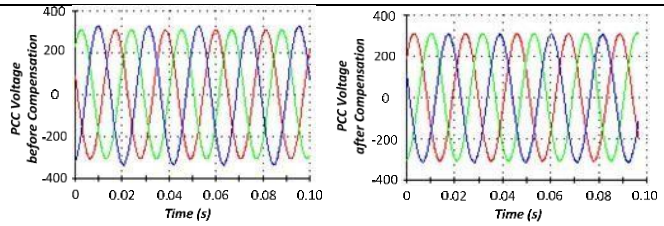

Fig. 14. *PCC* voltage unbalance factor.

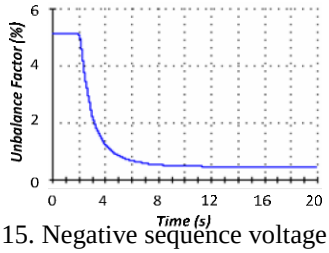

Fig. 15. Negative sequence voltage of *PCC*.

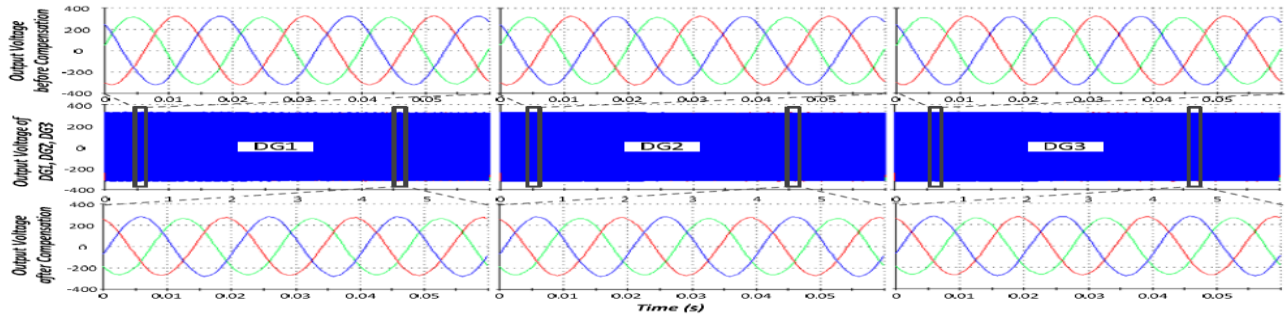

Fig. 16. Ourput voltage of DG1, DG2, and DG3.

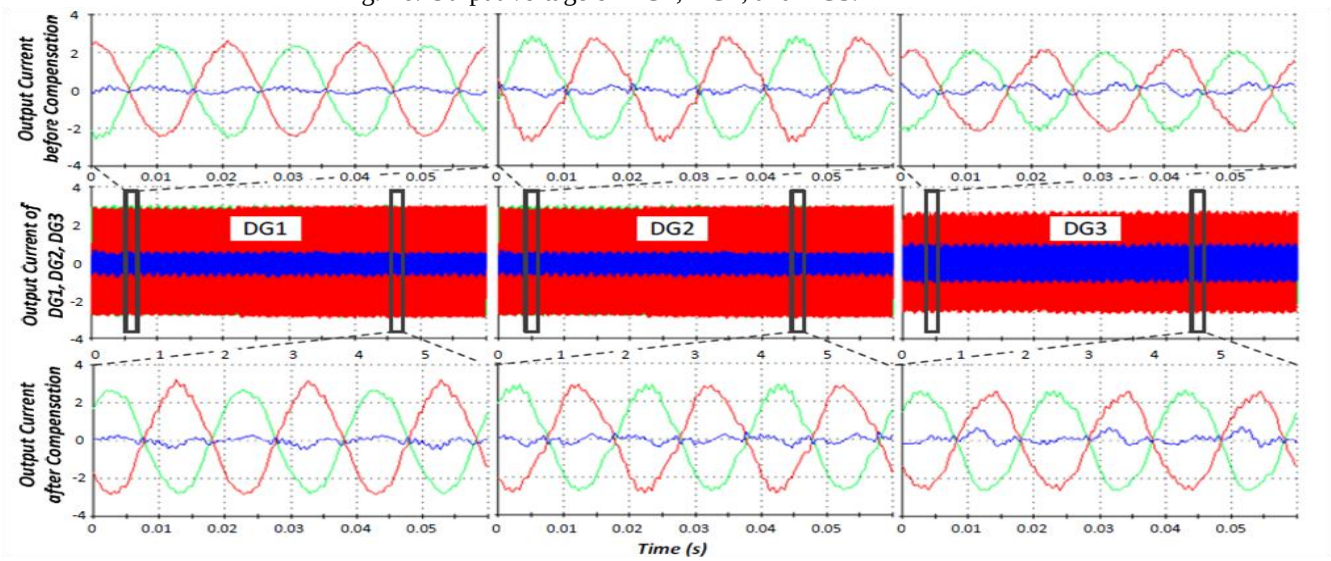

Fig. 17. Ourput current of DG1, DG2, and DG3.

Moreover, in order to investigate the current sharing accuracy, the output current of the three DGs before and after the compensation is depicted in Fig. 17. As it can be seen, the output current can be shared properly among the three DG converters. Also, it is worth noting that the current errors between the three DG converters are caused by the difference in line impedance.

4.CONCLUSIONS

In this paper, a novel direct voltage unbalance compensation control strategy for islanded microgrids has been investigated. The control structure includes two levels: a local controller and an direct voltage unbalance compensator. The local controller mainly takes care of the bus voltage regulation and the power sharing

accuracy, while the direct voltage unbalance compensator contributes to mitigate the voltage unbalance at the *PCC* by controlling the voltage reference. The effectiveness of the control scheme has been validated with three *LCL* DG converters connected in parallel sharing a common AC bus. The experimental results show that the negative sequence voltage can be well suppressed to the desired value with a satisfied load sharing accuracy.

REFERENCES

[1] H. Nikkhajoei and R.H. Lasseter, "Distributed generation interface to the CERTS microgrid," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1598- 1608, Jul. 2009.

[2] Y. Xu, L.M. Tolbert, J. D. Kueck, and D.T. Rizy, "Voltage and current unbalance compensation using a static var compensator," *IET on Power Electron.*, vol. 3, no. 6, pp.977-988, Nov. 2010.

[3] P. S. Flannery, G. Venkataramanan, "Unbalanced voltage sag ride- through of a doubly fed induction generator wind turbine with series grid-side converter," *IEEE Trans. on Ind. Appl.*, vol. 45, no. 5, pp. 1879- 1887, Sep.-Oct. 2009.

[4] Y. Xu; L. M. Tolbert, and J. D. Kueck, "Voltage and current unbalance compensation using a parallel active filter," *IEEE Power Electron. Spec. Conf.*, pp. 2919-2925, June 2007.

[5] M. Hojo, Y. Iwase, T. Funabashi, and Y. Ueda, "A method of three- phase balancing in microgrid by photovoltaic generation systems," *IEEE Power Electron. and Motion Control Conf.*, pp. 2487-2491, Sep. 2008.

[6] M. Savaghebi, A. Jalilian, J. C. Vasquez, J. M. Guerrero, "Autonomous voltage unbalance compensation in an islanded droop-controlled microgrid," *IEEE Trans. on Ind. Electron.*, vol. 60, no. 4, pp. 1390- 1402, April 2013.

[7] R. Teodorescu, F. Blaabjerg, M. Liserre and P. C. Loh. "Proportional resonant controllers and filters for grid-connected voltage-source

$$v_c(s) = v_o^*(s) - Z_o(s) i_o(s) =$$

$$\frac{G_v(s) G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} v_{ref}(s) -$$

$$\frac{Ls + G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} i_o(s)$$

$$v_c(s) = v_o^*(s) - Z_o(s) i_o(s) =$$

$$\frac{G_v(s) G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} v_{ref}(s) -$$

$$\frac{Ls + G_i(s) G_{PWM}(s)}{LCs^2 + CG_i(s) G_{PWM}(s) s + G_v(s) G_i(s) G_{PWM}(s) + 1} i_o(s)$$