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Intermittency Smoothing and Improving Power Quality Distribution Grid using An Ultra capacitor (UCAP) Integrated Power Conditioner

K.Kalpana [1], V.N. Saraswathi[2]
[1](EEE Depat.,SVPCET,puttor,India)
[2](EEE Depat.,SVPCET,puttor,India)

Abstract: Penetration of various types of distributed energy resources (DERs) like solar, wind, and plug-in hybrid electric vehicles (PHEVs) onto the distribution grid is on the rise. There is a corresponding increase in power quality problems and intermittencies on the distribution grid. In order to reduce the intermittencies and improve the power quality of the distribution grid, an ultra capacitor (UCAP) integrated power conditioner is proposed in this paper. UCAP integration gives the power conditioner active power capability, which is useful in tackling the grid intermittencies and in improving the voltage sag and swell compensation. UCAPs have low energy density, high-power density, and fast charge/discharge rates, which are all ideal char-acteristics for meeting high-power low-energy events like grid intermittencies, sags/swells. In this paper, UCAP is integrated into dc-link of the power conditioner through a bidirectional dc–dc converter that helps in providing a stiff dc-link voltage. The integration helps in providing active/reactive power support, intermittency smoothing, and sag/swell compensation. Design and control of both the dc–ac inverters and the dc–dc converter are discussed. The simulation model of the overall system is developed and compared with the experimental hardware setup.

Index Terms: Active power filter (APF), dc–dc converter, d–q control, digital signal processor (DSP), dynamic voltage restorer (DVR), energy storage integration, sag/swell, ultra capacitors (UCAP).

I INTRODUCTION

POWER QUALITY is major cause of concern in the in-dustry, and it is important to maintain good power quality on the grid. Therefore, there is renewed interest in power quality products like the dynamic voltage restorer (DVR) and active power filter (APF). DVR prevents sensitive loads from experiencing voltage sags/swells [1], [2], and APF prevents the grid from supplying nonsinusoidal currents when the load is nonlinear [3]. The concept of integrating the DVR and APF through a back–back inverter topology was first introduced in [4] and the topology was named as unified power quality conditioner (UPQC). The design goal of the traditional UPQC was limited to improve the power quality of the distribution grid by being able to provide sag, swell, and harmonic current compensation. In this paper, energy storage integration into the power conditioner topology is being proposed, which will allow the integrated system to provide additional functionality.

With the increase in penetration of the distribution energy resources (DERs) like wind, solar, and plug-in hybrid electric vehicles (PHEVs), there is a corresponding increase in the power quality problems and intermittencies on the distribution grid in the *seconds* to *minutes* time scale [5]. Energy storage integration with DERs is a potential solution, which will increase the reliability of the DERs by reducing the intermittencies and also aid in tackling some of the power quality problems on the distribution grid [5]–[8]. Applications where energy storage integration will improve the functionality are being identified, and efforts are being made to make energy storage integration commercially viable on a large scale [9], [10]. Smoothing of DERs is one application where energy storage integration and optimal control play an important role [11]. In [11], super capacitor and flow battery hybrid energy storage system are integrated into the wind turbine generator to provide wind power smoothing, and the system is tested using a real-time simulator. In [12], super capacitor is used as an auxiliary energy storage for photovoltaic (PV)/fuel cell, and a model-based controller is developed for providing optimal control. In [13], a battery energy storage system-based control to mitigate wind/PV fluctuations is proposed. In [14], multiobjective optimization method to integrate battery storage for improving PV integration into the distribution grid is proposed. In [15], a theoretical analysis is performed to determine the upper and lower bounds of the battery size for grid-connected PV systems. In , a rule-based control is proposed to optimize the battery discharge while dispatching intermittent renewable resources. In , optimal sizing of a zinc bromine-based energy storage system for reducing the intermittencies in wind power is proposed.

It is clear from the literature that renewable intermittency smoothing is one application that requires active power support from energy storage in the *seconds* to *minutes* time scale [10]. Reactive power support is another application which is gaining wide recognition with proposals for reactive power pricing. Voltage sag and swells are power quality problems on distribution grid that have to be mitigated. sag/swell compensation needs active power support from the energy

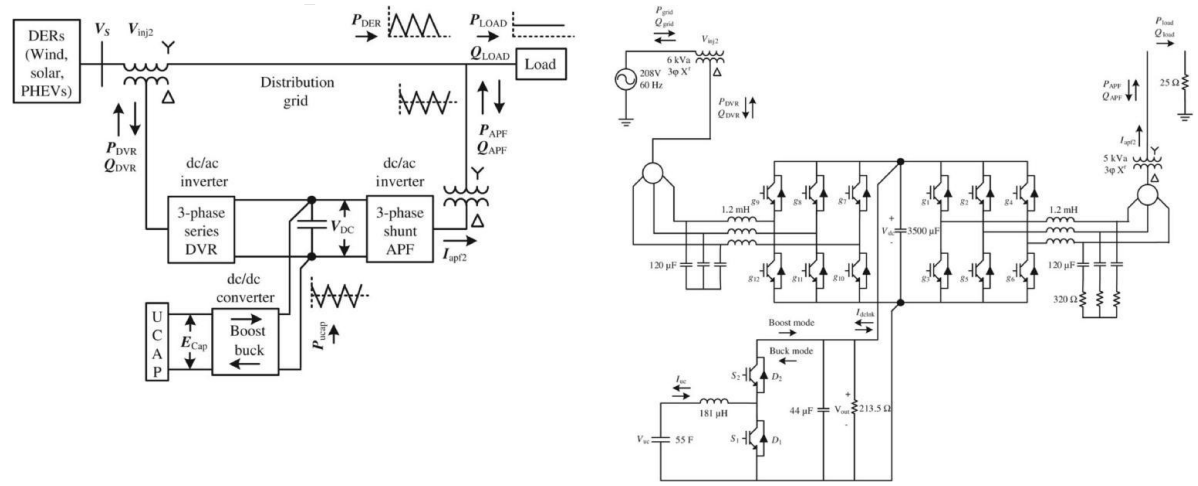


Fig. 1. One-line diagram of power conditioner with UCAP energy storage.

storage in the *milliseconds* to *1 min* duration [11]. All the above functionalities can be realized by integrating energy storage into the grid through a power conditioner topology. Of all the rechargeable energy storage technologies super-conducting magnet energy storage (SMES), flywheel energy storage system (FESS), battery energy storage system (BESS), and ultracapacitors (UCAPs), UCAPs are ideal for providing active power support for events on the distribution grid which require active power support in the *seconds* to *minutes* time scale like voltage sags/swells, active/reactive power support, and renewable intermittency smoothing [7].

In this paper, UCAP-based energy storage integration through a power conditioner into the distribution grid is proposed, and the following application areas are addressed.

1) Integration of the UCAP with power conditioner system gives the system *active power capability*.
2) *Active power capability* is necessary for independently compensating voltage sags/swells and to provide ac-tive/reactive power support and intermittency smoothing to the grid.
3) Experimental validation of the UCAP, dc–dc converter, inverter their interface, and control.
4) Development of inverter and dc–dc converter controls to provide sag/swell compensation and active/reactive support to the distribution grid.
5) Hardware integration and performance validation of the integrated UCAP-PC system.

II THREE-PHASE INVERTERS

A. Power Stage

The one-line diagram of the system is shown in Fig. 1. The power stage consists of two back-to-back three-phase voltage source inverters connected through a dc-link capacitor. UCAP energy storage is connected to the dc-link capacitor through a bidirectional dc–dc converter. The series inverter is respon-sible for compensating the voltage sags and swells; and the shunt inverter is responsible for active/reactive power support and renewable intermittency smoothing. The complete circuit diagram of the series DVR, shunt APF, and the bidirectional dc–dc converter is shown in Fig. 2. Both the inverter systems consist of IGBT module, its gate-driver, LC filter, and an isolation transformer. The dc-link voltage V_{dc} is regulated at 260 V for optimum voltage and current compensation of the converter and the line–line voltage V_{ab} is 208 V.

The goal of this project is to provide the integrated power conditioner and UCAP system with active power capability 1) to compensate *temporary voltage sag* (0.1–0.9 p.u.) and *swell* (1.1–1.2 p.u.), which last from 3 s to 1 min and 2) to provide active/reactive support and renewable intermittency smoothing, which is in the *seconds* to *minutes* time scale

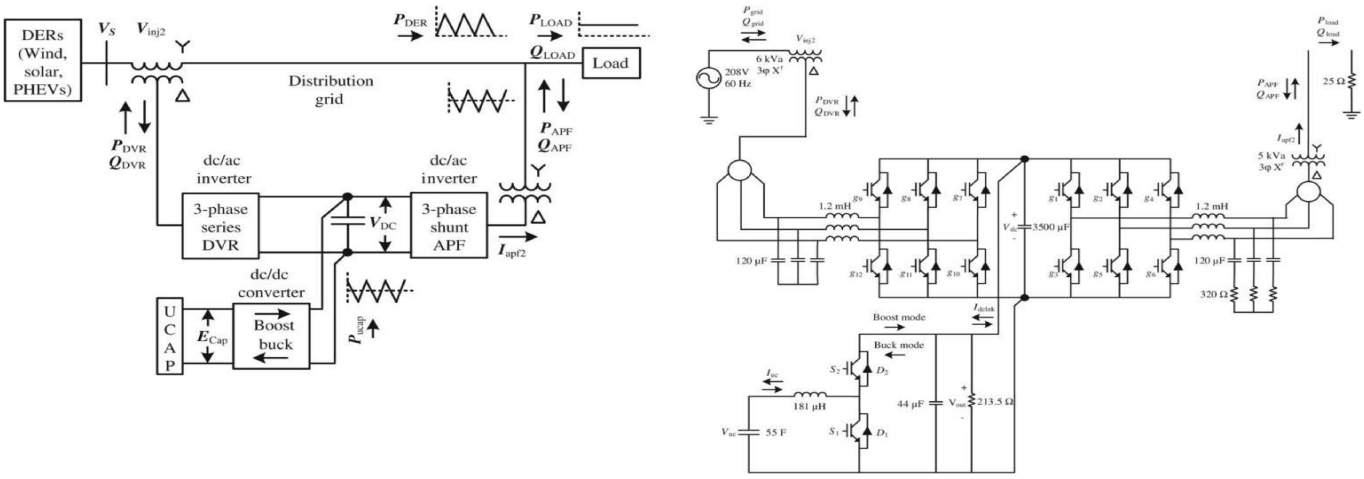


Fig. 2. Model of power conditioner with UCAP energy storage.

B. Controller Implementation

The series inverter controller implementation is based on the *in-phase compensation* method that requires PLL for estimating θ, and this has been implemented using the *fictitious power method* described in [4]. Based on the estimated θ and the line–line source, voltages V_{ab}, V_{bc}, V_{ca} (which are available for this delta-sourced system) are transformed into the d–q domain and the line–neutral components of the source voltage V_{sa}, V_{sb}, and V_{sc} which are not available can then be estimated using

$$\begin{bmatrix} V_{sb} \\ V_{sa} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} -\frac{2}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ 1 & 0 \\ -\frac{2}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \sin\theta\sin\frac{\pi}{6} - \cos\theta\cos\frac{\pi}{6} & \sin\theta\cos\frac{\pi}{6} + \cos\theta\sin\frac{\pi}{6} \\ \sin\theta & -\cos\theta \end{bmatrix} \begin{bmatrix} V_q \\ V_d \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_{refb} \\ V_{refa} \\ V_{refc} \end{bmatrix} = m \begin{bmatrix} \sin\left(\theta - \frac{2\pi}{3}\right) \\ \sin\theta \\ \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \frac{V_{sa}}{V_s} \quad (2)$$

$$P_{dvr} = 3V_{inj2a(rms)} I_{La(rms)} \cos\phi$$
$$Q_{dvr} = 3V_{inj2a(rms)} I_{La(rms)} \sin\phi. \quad (3)$$

These voltages are normalized to unit sine waves using
line–neutral system voltage of 120 V_{rms} as reference and compared with unit sine waves *in-phase* with actual system voltages V_s from (2) to find the injected voltage references V_{ref} necessary to maintain a constant voltage at the load terminals, where m is the modulation index, which is 0.45 for this case. Therefore, whenever there is a voltage sag or swell on the source side, a corresponding voltage V_{inj2} is injected in-phase by the DVR and UCAP system to negate the effect and retain a constant voltage V_L at the load end. The actual active and reactive power supplied by the series inverter can be computed using (3) from the rms values of injected voltage V_{inj2a} and load current I_{La} and ϕ is the phase difference between the two waveforms

$$P_{ref} = -3 V_{sq} I_{qref} \quad (4)$$

$$Q_{ref} = -\frac{3}{2} V_{sq} I_{dref}$$

$$\begin{bmatrix} i_{refa} \\ i_{refb} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \quad (5)$$

$$i_{refc} = -\frac{1}{2} - \frac{\sqrt{3}}{2}$$

The shunt inverter controller implementation is based on the $i_d - i_q$ method, which is modified to provide active and reactive power compensation, such that i_d controls the reactive power and i_q controls the active power. Therefore, based on the references for active and reactive powers P_{ref} and Q_{ref}, the reference currents i_{qref} and i_{dref} in d–q domain can be calculated using (4), where v_{sq} is the system voltage in q-domain and the reference currents are calculated using (5). The complete inverter control algorithm is implemented in the DSP TMS320F28335, which has a clock frequency of 150 MHz, an inbuilt A/D module, PWM module, and real-time emulation, which are all ideal for this application.

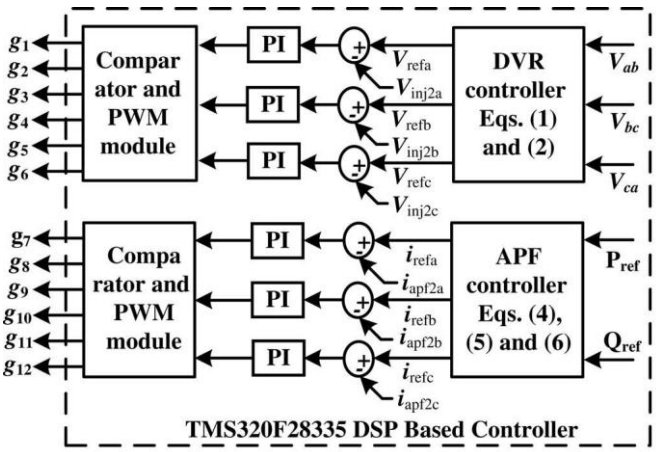


Fig. 3. Controller block diagram for DVR and APF.

Assuming that the UCAP bank can be discharged to 50% of its initial voltage ($V_{uc,ini}$) to final voltage ($V_{uc,fin}$) from 144 to 72 V, which translates to depth of discharge of 75%, the energy in the UCAP bank available for discharge is given by

$$E_{UCAP} = \frac{1}{2} * C * \frac{(V_{uc,ini}^2 - V_{uc,fin}^2)}{60} \text{ W min}$$

$$E_{UCAP} = \frac{1}{2} * 165 * \frac{144^2 - 72^2}{60} = 7128 \text{ W min.} \quad (6)$$

B. Bidirectional DC–DC Converter and Controller

A bidirectional dc–dc converter is required as an interface between the UCAP and the dc-link, since the UCAP voltage varies with the amount of energy discharged, while the dc-link voltage has to be stiff. The model of the bidirectional dc–dc converter and its controller are shown in Fig. 4(a). The dc–dc converter should operate in *Discharge* mode, while providing

III. UCAP AND BIDIRECTIONAL DC–DC CONVERTER

A. UCAP Bank Hardware Setup

UCAPs can deliver very high power in a short time span; they have higher power density and lower energy density when compared with Li-ion batteries. The major advantage UCAPs have over batteries is their power density characteristics, high number of charge–discharge cycles over their lifetime, and higher terminal voltage per module [5], These are ideal characteristics for providing active/reactive power support and intermittency smoothing to the distribution grid on a *short-term* basis. In it is proposed that UCAPs are currently viable as short-term energy storage for bridging power in kilowatt range in the *seconds* to *few minutes* timescale. The choice of the number of UCAPs necessary for providing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage, and distribution grid voltages. For a 260-V dc-link voltage, it is practical and cost-effective to use three modules in the UCAP bank. Therefore, in this paper, the experimental setup consists of three 48 V, 165 F UCAPs (BMOD0165P048) manufactured by Maxwell Technologies, which are connected in series. active/reactive power support and voltage sag compensation. The dc–dc converter should also be able to operate in bidirectional mode to be able to *charge* or absorb additional power from the grid during intermittency smoothing. In this paper, the bidirectional dc–dc converter acts as a boost converter, while *discharging* power from the UCAP and acts as a buck converter while *charging* the UCAP from the grid.

Average current mode control, which is widely explored in literature, is used to regulate the output voltage of the bidirectional dc–dc converter in both *Buck* and *Boost* modes while *charging* and *discharging* the UCAP bank. This method tends to be more stable when compared with other methods like voltage mode control and peak current mode control. Average current mode controller is shown in Fig. 3, where the actual output voltage V_{out} is compared with the reference voltage V_{ref} and the error is passed through the voltage compensator $C_1(s)$ that generates the average reference current I_{ucref}.

C. Controller Implementation

Average current mode control is used to regulate the output voltage of the bidirectional dc–dc converter in both *Buck*

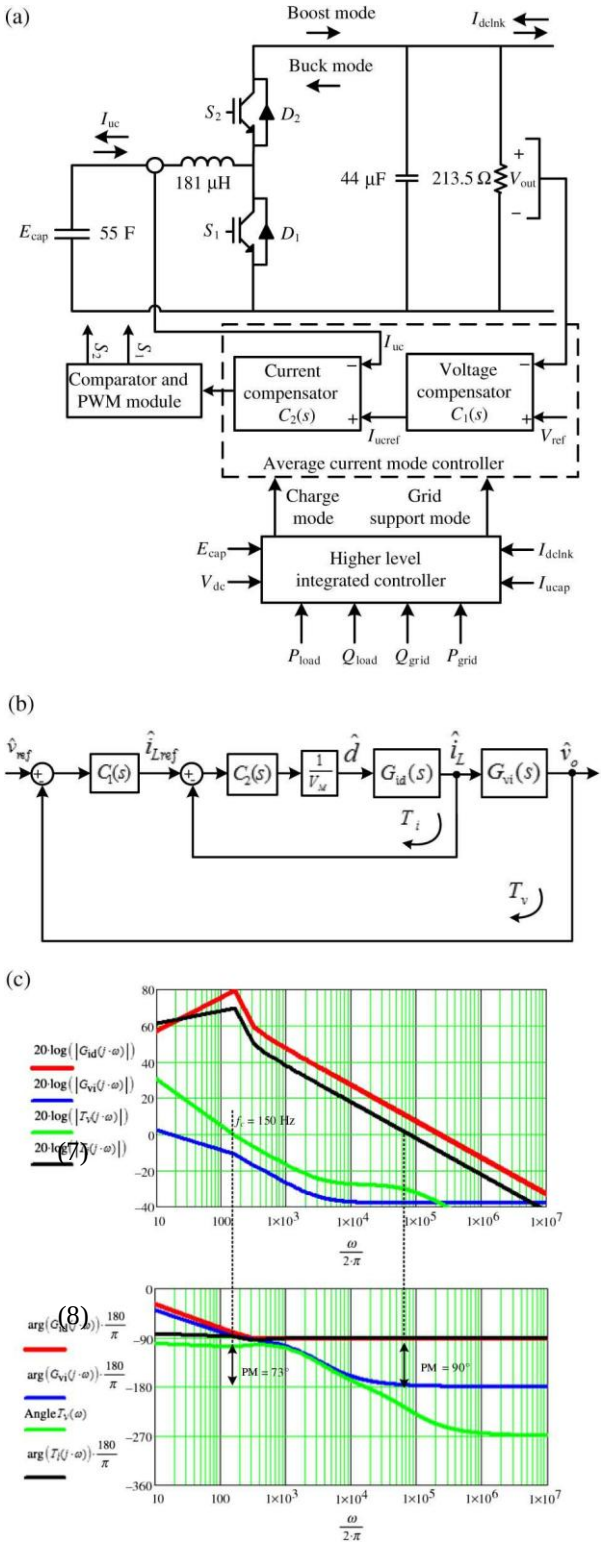
and *Boost* modes, while *charging* and *discharging* the UCAP bank. While the UCAP-APF system is *discharging* power, the dc-link voltage V_{out} tends to be less than V_{ref} , which causes the reference current I_{ucref} to be positive, thereby operating the dc–dc converter in *Boost mode*. Along similar lines, when the UCAP-APF system is absorbing power from the grid, the dc-link voltage V_{out} tends to be greater than V_{ref} , which causes the reference current I_{ucref} to be negative and thereby operating the dc–dc converter in *Buck mode*. Average current mode control technique is widely explored in the literature [19], and it was found as the ideal method for UCAP-APF integration as it tends to be more stable when compared with other methods like voltage mode control and peak current mode control. This is a major advantage in the present topology, where the stability of the dc–dc converter has to be ensured over a wide operating range and in both *Buck* and *Boost* modes of operation. Average current mode controller and the higher level integrated controller are shown in Fig. 4(a), where the actual output voltage V_{out} is compared with the reference voltage V_{ref} and the error is passed through the voltage compensator $C_1(s)$, which generates the average reference current I_{ucref} . This is then compared with the actual UCAP current (which is also the inductor current) I_{uc}, and the error is then passed through the current compensator $C_2(s)$.

The converter model for average current mode control is based on the following transfer functions developed in [19]:

$$G_{id}(s) = \frac{V_{out}\left(sC + \frac{2}{R}\right)}{s^2LC + sRL + (1-D)^2} \quad (7)$$

$$G_{vi}(s) = \frac{(1-D)\left(1 - \frac{sL}{R(1-D)^2}\right)}{sC + \frac{2}{R}} \quad (8)$$

The model of the dc–dc converter in average current mode control is shown in Fig. 4(b) that has two loops. The inner current loop $T_i(s)$ has the current compensator $C_2(s)$, voltage modulator gain V_M , and the transfer function $G_{id}(s)$. The outer voltage loop $T_V(s)$ constitutes the voltage compensator $C_1(s)$, current loop $T_i(s)$, and the transfer function $G_{vi}(s)$. The current compensator design $C_2(s)$ must be carried out initially and the voltage compensator $C_1(s)$ design is based on the design of the current



compensator due to the dependency of $C_1(s)$ on $C_2(s)$. The current compensator $C_2(s)$ must be designed in such a way that at the crossover frequency of the current loop there is enough phase-margin to make the current loop $T_i(s)$ stable and it should have a higher bandwidth when compared to the voltage loop $T_V(s)$. Based on these criteria, the transfer functions of the current loop $T_i(s)$ and the current compensator $C_2(s)$ are given by

$$\frac{C_2(s)}{T_i(s)} = G_{id}(s) \cdot \frac{1}{V_M} \quad (9)$$

$$C_2(s) = 1.67 + \frac{231.81}{s}. \quad (10)$$

Fig. 4. (a) Model of the bidirectional dc–dc converter and its controller. (b) Model of the dc–dc converter in average current mode control. (c) Bode plot of various transfer functions.

The closed-loop transfer function of the current loop is then given by

$$T_1(s) = \frac{T_i(s)}{1 + T_i(s)}. \quad (11)$$

It can be observed from Fig. 4(c) that the phase margin is around 90° at the crossover frequency of the current loop $T_i(s)$, and it has higher bandwidth when compared with the voltage loop $T_V(s)$. The voltage loop compensator $C_1(s)$ design is dependent on the design of $T_1(s)$, and it is a PI compensator whose gain is adjusted to have the desired crossover frequency. Based on these criteria, the transfer functions of the voltage loop $T_V(s)$ and compensator $C_1(s)$ is given by

$$T_V(s) = G_{vi}(s)\, C_1(s)\, T_1(s) \quad (12)$$

$$C_1(s) = 3.15 + \frac{1000}{s}. \quad (13)$$

The transfer function of the plant $G_{vi}(s)$ along with the transfer function of $C_1(s)$ of the voltage compensator and the overall voltage loop transfer function $T_V(s)$ are shown in Fig. 4(c). It can be observed that the voltage loop $T_V(s)$ has a crossover frequency of around 150 Hz with a phase margin of 73°, which provides a stable dynamic response. The stability and dynamic performance of the voltage loop $T_V(s)$ determine the stability and dynamic response of the overall system.

D. Higher Level Integrated Controller

The higher level integrated controller is designed to make system level decisions on the inverter and dc–dc converter controllers. Based on various system parameters like P_{load}, Q_{load}, P_{grid}, Q_{grid}, V_{ucap}, V_{dc}, I_{dclnk}, and I_{ucap}, the higher level integrated controller will decide on operating in one of the following modes: *active power support mode*, *reac-tive power support mode*, *renewable intermittency smooth-ing mode*, *sag/swell compensation mode*, and *UCAP charge mode*.

In *active power support mode* and *renewable intermittency smoothing mode*, the UCAP-PC system must provide active power to the grid. Therefore, the active power capability of the UCAP-PC system must be assessed by the higher level integrated controller. Based on the P_{grid} and P_{load} values, the reference P_{ref} is calculated in the higher level integrated controller, and it will decide if the UCAP has enough energy to respond to the P_{ref} command based on the UCAP state of charge. If the UCAP has enough capacity to respond to the request, then the dc–dc converter controller is operated in *grid support mode*; otherwise, it is operated in *charge mode*, where the UCAP is recharged and the power request is met at a later time. In grid support mode, the dc–dc converter will operate in a bidirectional fashion in both Buck and Boost modes to respond to the active power requests and regulate the dc-link voltage in a stable fashion, while the inverter controller should respond such that the commanded P_{ref} is supplied by the inverter through current control.

In *reactive power support mode*, the UCAP-PC system must provide reactive power to the grid. In this mode, the UCAP-PC does not provide any active power to the grid and even the PC losses are supplied by the grid. Based on the Q_{grid} and Q_{load} values, the reference Q_{ref} is calculated in the higher level integrated controller. In this mode, the dc–dc converter controller can be programmed to operate in *grid support mode* directly because the active power requirement for operating in this mode is minimal. Therefore, the goal of the dc–dc converter controller is to regulate the dc-link voltage in a stable fashion, while the inverter controller should respond

such that the commanded Q_{ref} is supplied by the inverter through current control.

In *sag/swell compensation mode*, the UCAP-PC system is programmed to prevent sensitive loads from disturbances on the supply-side like voltage sag or voltage swell. These disturbances require short-term energy storage, and in this mode, the dc–dc converter controller can be programmed to operate in *grid support mode*. Therefore, the goal of the dc–dc converter controller is to regulate the dc-link voltage in a stable fashion during both sag/swell events. It is also required that the dc–dc converter be able to *discharge* and meet the active power requirements during a voltage sag and to be able absorb active power in a stable fashion during a voltage swell event.

In *charge mode*, the UCAP is recharged by absorbing active power from the grid when the UCAP state of charge falls below 50%. The rate at which the UCAP can be charged is assessed by the higher level integrated controller based on the P_{grid} and P_{load} values and the reference P_{ref} is calculated. Then the dc–dc converter controller is commanded to operate in *charge mode*, wherein the dc–dc converter will operate in Buck Mode to absorb the power from the grid and the inverter controller must respond to supply commanded P_{ref} .

IV. SIMULATION RESULTS

The simulation of the proposed UCAP integrated power conditioner system is carried out in PSCAD for a 208-V, 60-Hz system, where 208 V is 1 p.u. The system response for a three-phase voltage sag which lasts for 0.1 s and has a depth of 0.64 p.u. is shown in Fig. 5(a)–(e). It can be observed from Fig. 3 (a) that during voltage sag, the source voltage V_{srms} is reduced to 0.36 p.u., while the load voltage V_{Lrms} is maintained constant at around 1.01 p.u. due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line–line source voltages (V_{sab}, V_{sbc}, and V_{sca}) [Fig. 5(b)], the line–line load voltages (V_{Lab}, V_{Lbc}, and V_{Lca}) [Fig. 5(c)], and the line–neutral injected voltages of the series inverter (V_{inj2a}, V_{inj2b}, and V_{inj2c}) [Fig. 5(d)]. In Fig. 6(a), the plots of the bidirectional dc– dc converter are presented, and it can be observed that the dc-link voltage V_{fdc} is regulated at 260 V, the average dc-link current $I_{dclnkav}$ and the average UCAP current I_{ucav} increase to provide the active power required by the load during the sag. This can also be observed from various active power plots shown in Fig. 6(b), where the power supplied to the load P_{load} remains constant even during the voltage sag when the grid power P_{grid} is decreasing. The active power deficit of the grid is met by the DVR power P_{dvr}, which is almost equal to the input power to the inverter $P_{dc\ in}$
available from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and load during the voltage sag event is being met by the UCAP-based energy storage system through bidirectional dc–dc converter and the inverter. It can also be noticed that the grid reactive power Q_{grid} reduces during the voltage sag while Q_{dvr} increases to compensate for the reactive power loss in the system. Similar analysis can also be carried out for voltage

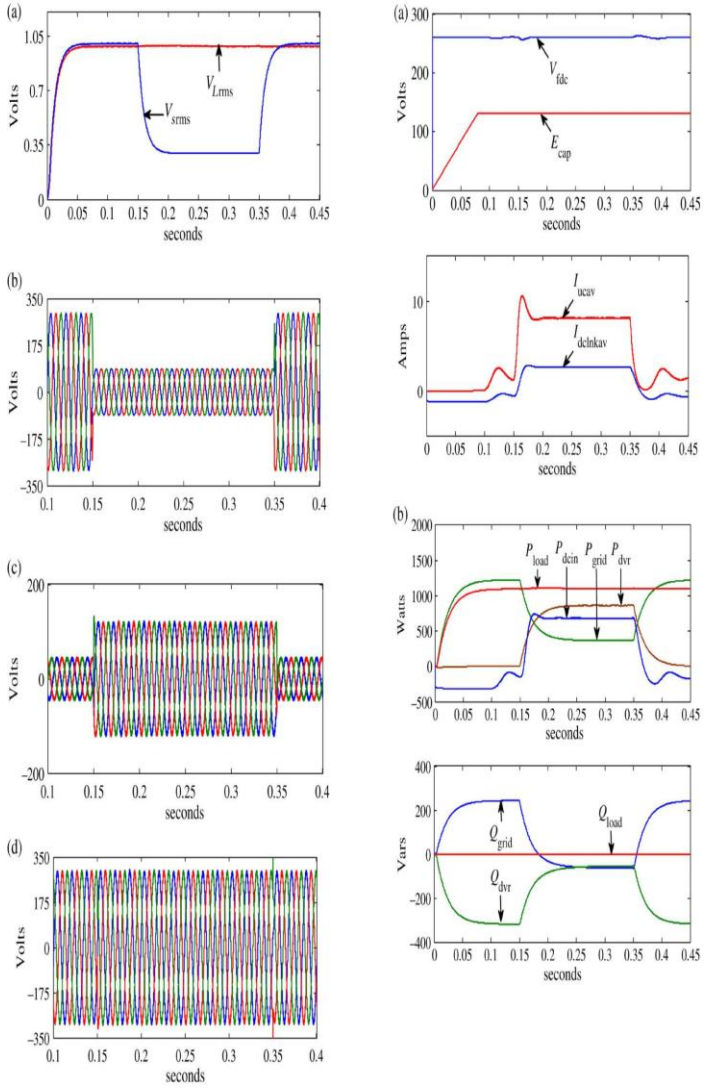


Fig. 5. (a) Source and load rms voltages V_{srms} and V_{Lrms} during sag.
(b) Source voltages V_{sab} (blue), V_{sbc} (red), and V_{sca} (green) during sag.
(c) Injected voltages V_{inj2a} (blue), V_{inj2b} (red), and V_{inj2c} (green) during sag. (d) Load voltages V_{Lab} (blue), V_{Lbc} (red), and V_{Lca} (green) during sag.

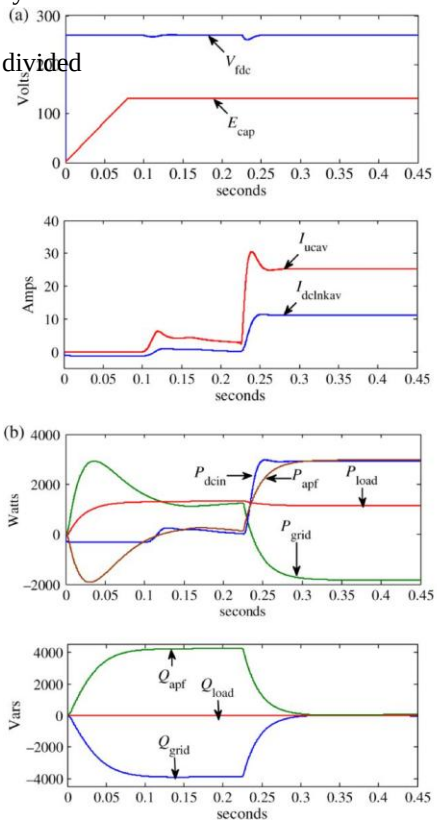
Fig. 6. (a) Currents and voltages of dc–dc converter. (b) Active and reactive power of grid, load, and inverter during voltage sag.

sags that occur in one of the phases (A, B, or C) or in two of the phases (AB, BC, or CA); however, three-phase voltage sag case requires the maximum active power support and is presented here.

The proposed UCAP integrated power conditioner system's performance is then simulated for the active and reactive power support case. The system response is simulated for the reactive power support mode for the initial 0.225 s, where i_{dref} = −15 A for the initial 0.225 s, which translates to a of Q_{ref}= 3819 Var from (4). For the rest of the 0.225 s, the system response is simulated for active power support mode with i_{qref} = −12A, which translates to P_{ref} of 3054 W. It can be observed from the currents and voltages of the dc–dc converter waveforms in Fig. 7(a) that the dc-link voltage V_{fdc} stays constant in both the modes. While the UCAP current I_{ucav} and the corresponding dc-link current $I_{dclnkav}$ are higher for active power support case when compared with the reactive power support case. In Fig. 7(b), the active and reactive power curves for both the modes are presented, and it can be observed from the active and reactive power curves that the reactive power Q_{apf} reaches the commanded value in the reactive power support mode and the active power P_{dcin} supplied by the UCAP is minimal in this case. In the active power support mode, the UCAP and the inverter system supply the required active power and the additional power flows back into the grid. This can be observed from the P_{dcin}, P_{grid}, P_{load}, and P_{apf} waveforms.

V. EXPERIMENTAL RESULTS

In order to iverify the concept and simulation results experimentally, a hardware prototype of the complete sys-tem was constructed and is shown in Fig. 8(a) and (b). In Fig. 8(a), the complete inverter system that is divided



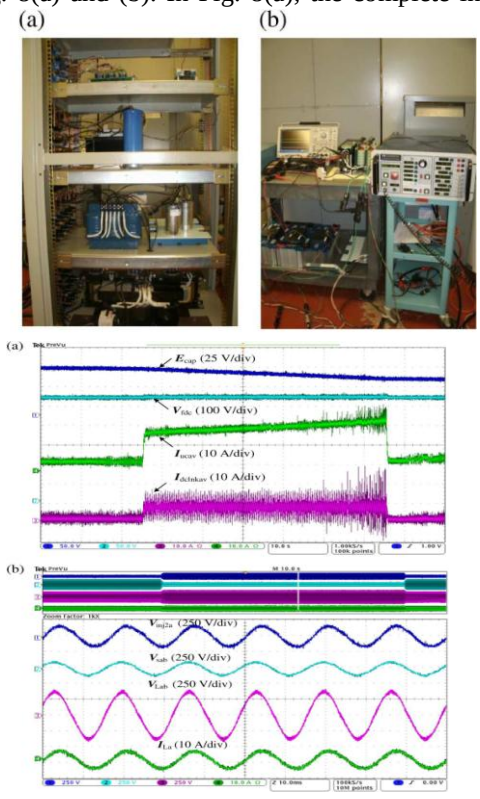


Fig. 7. (a) Currents and voltages of bidirectional dc–dc converter for i_{dref} **= −15.0 A** (reactive power support) and i_{qref} **= −12.0 A** (active power support). (b) Grid, load, and inverter active and reactive power curves for i_{dref} **= −15.0 A** (reactive power support) and i_{qref} **= −12.0 A** (active power support).

Fig. 8. (a) Sensor, interface, and DSP boards (first), dc-link capacitor and inverters (second), LC filters (third), and isolation transformers (fourth).
(b) DC–DC converter and MSO4034B oscilloscope (top shelf), UCAP bank with three UCAPs (bottom shelf) and the industrial power corruptor

into four shelves is shown. The topmost shelf consists of a sensor board, an interface board, TMS320F28335 DSP controller, and their power supply circuit. The second shelf consists of the series and shunt inverters connected back– back through a dc-link capacitor. Each inverter consists of an IGBT module (BSM100GD60DLC) which is a 600-V 100 A six-pack module from Infineon, and its gate driver SKHI 61R manufactured by SEMIKRON, and the inverters are connected back–back through a 3500-μF 450 Vdc dc-link capacitor; the third shelf has the LC-filters of the series and the shunt inverters. The LC filter of the shunt inverter consists of 1.2 mH 45-A three-phase inductor and three 120 μF 240-Vac capacitors connected in wye configuration through 320 Ω damping resistors. The series inverter LC filter consists of another 1.2 mH 45-A three-phase inductor and three-phase 2.5 kVar capacitors connected in delta configuration. The fourth shelf consists of three 2-kVa 125 V/50 V single-phase isolation transformers for the series inverter connected in delta

Fig. 9. (a) UCAP and bidirectional dc–dc converter experimental waveforms
E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3), and I_{ucav} (CH4) during voltage sag compensation by series inverter. (b) Series inverter experimental wave-
forms V_{sab} (CH1), V_{Lab} (CH2), and V_{inj2a} (CH3) and I_{La} (CH4) during the voltage sag.

configuration on the primary side and the secondary sides are connected in series with the grid through a protection circuit breaker. The fourth shelf also has a 5-kVA $-Y$ iso-lation transformer for the shunt inverter, where the secondary

side is connected to the grid through a protection circuit breaker. In Fig. 8(b), the UCAP, the bidirectional dc–dc converter, the oscilloscope, and the industrial power corruptor are shown.

In Fig. 9(a) and (b), the experimental waveforms of the series inverter and the bidirectional dc–dc converter are shown for the case where the grid experiences voltage sag of 0.6 p.u. magnitude for 1 min duration. In Fig. 9(a), the dc-link voltage V_{fdc} (CH1), the UCAP voltage E_{cap} (CH2), the dc-link current

(CH3), and the average UCAP current I_{ucav} (CH4)

I_{dclnk}

are shown. It can be observed from Fig. 9(a) that during the voltage sag, E_{cap} is decreasing rapidly and I_{ucav} is increasing rapidly; while V_{fdc} and $I_{dclnkav}$ are constant. Therefore, the dc–dc converter is able to regulate the dc-link voltage to 260 V and operate in *Boost* mode to discharge active power during a voltage sag event to meet the active power deficit between the grid and the load. In Fig. 9(b), the zoomed in versions of the line–neutral injected voltage V_{inj2a} (CH1), line–line source voltage V_{Lab} (CH2), the line–line load voltage V_{Lab} (CH1), and the load current I_{La} (CH4) during the voltage sag event are shown. It can be observed that during the voltage sag event the magnitude of V_{sab} is reduced while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a}, which increases during the voltage sag event to compensate for the voltage sag. Therefore, from both inverter and dc–dc converter experimental waveforms, it can be concluded that the UCAP integrated DVR system hard-ware setup is able to respond instantaneously to compensate voltage sags.

Similarly, in Fig. 10(a) and (b), the dc–dc converter and the inverter experimental waveforms are presented for the case where the grid experiences a voltage swell of 1.2 p.u. magnitude which lasts for 1 min duration. It can be ob-served from Fig. 10(a) that during the voltage swell E_{cap} is increasing slowly I_{ucav} and $I_{dclnkav}$ are negative while V_{fdc} stays constant. This indicates that the dc–dc converter is able to regulate the dc-link to 260 V and operate in *Buck* mode to charge the UCAP and absorb the additional power from the grid during the voltage swell into the UCAP, which also proves the bidirectional capability of the converter. It can be observed from Fig. 10(b) that during the voltage swell event the magnitude of V_{sab} has increased while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a}, which increases to compensate for the voltage swell. It can also be observed that the load current I_{La} is constant and in phase with the injected voltage V_{inj2a} which lags V_{sab} and V_{Lab} by 180°. Therefore, from the inverter and dc–dc converter experimental waveforms, it can be con-cluded that hardware setup is able to respond instantaneously to compensate voltages swells and operate in bidirectional mode.

In Fig. 11(a), the experimental waveforms of the bidi-rectional dc–dc converter are shown, which shows the full operation of the UCAP-PC system with the UCAP voltage

(CH1), the dc-link voltage V_{fdc} (CH2), the average

UCAP current I_{ucav} (CH3), and the dc-link current I_{dclnk} (CH4). Fig. 11(a) is divided into seven zones that are labeled from 1 through 7 in the plots. In zone 1, the inverter is

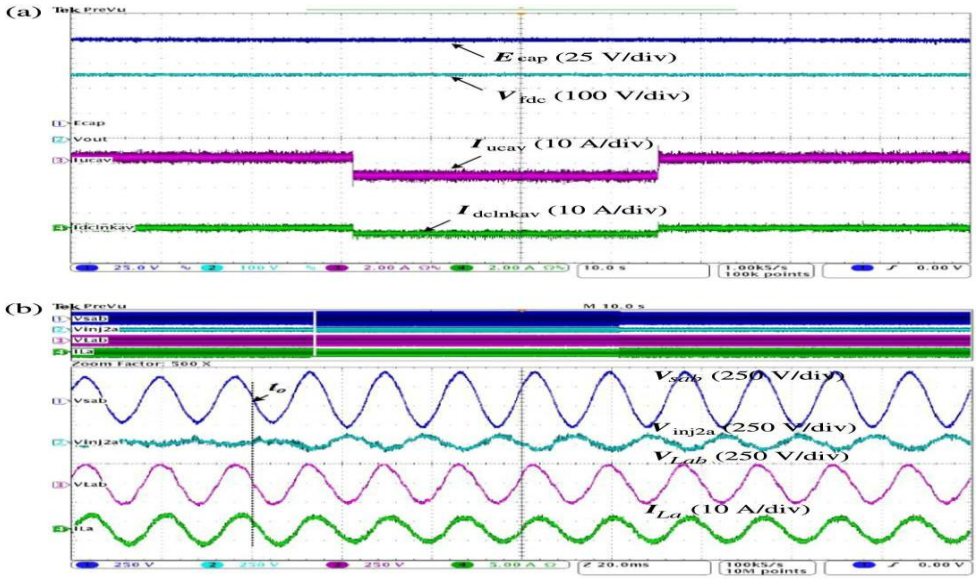


Fig. 10. (a) UCAP and bidirectional dc–dc converter experimental waveforms

E_{cap} (CH1), V_{fdc} (CH2), I_{dclnk} (CH3), and I_{ucav} (CH4) during voltage swell compensation by series inverter. (b) Series inverter experimental waveforms V_{sab} (CH1), V_{Lab} (CH2), and V_{inj2a} (CH3), and I_{La} (CH4) during the voltage swell.

supplying only reactive power and the dc–dc converter is maintaining a stiff dc-link voltage. Zone 2 is a transition mode in which the inverter is changing from supplying reactive power to active power. In zones 3–5, the inverter is supplying only active power to the grid, which is being discharged from the UCAP. In zones 4 and 5, the inverter is supplying only active power to the grid; however, the amount of active power supplied to the grid in zone 5 is less than that in zone 4 which is less than that in zone 3; this can be observed from I_{dclnk} trace. In zone 6, inverter is absorbing active power from the grid which is used for charging the UCAP through the bidirectional dc–dc converter. Zone 7 is again a transition mode in which the inverter is changing from supplying active power to supplying reactive power to the grid. In zone 8, again the inverter is supplying only reactive power to the grid and the dc–dc converter is maintaining a stiff dc-link voltage.

In Fig. 11(b), the zoomed in view of zone 1 is presented where the inverter is only providing reactive power support to the grid by commanding $i_{dref} = -10.0$ A and this can be concluded from the fact that I_{apf2a} is lagging V_{sa} by around 92°. Similarly, it can be noticed from zones 1 and

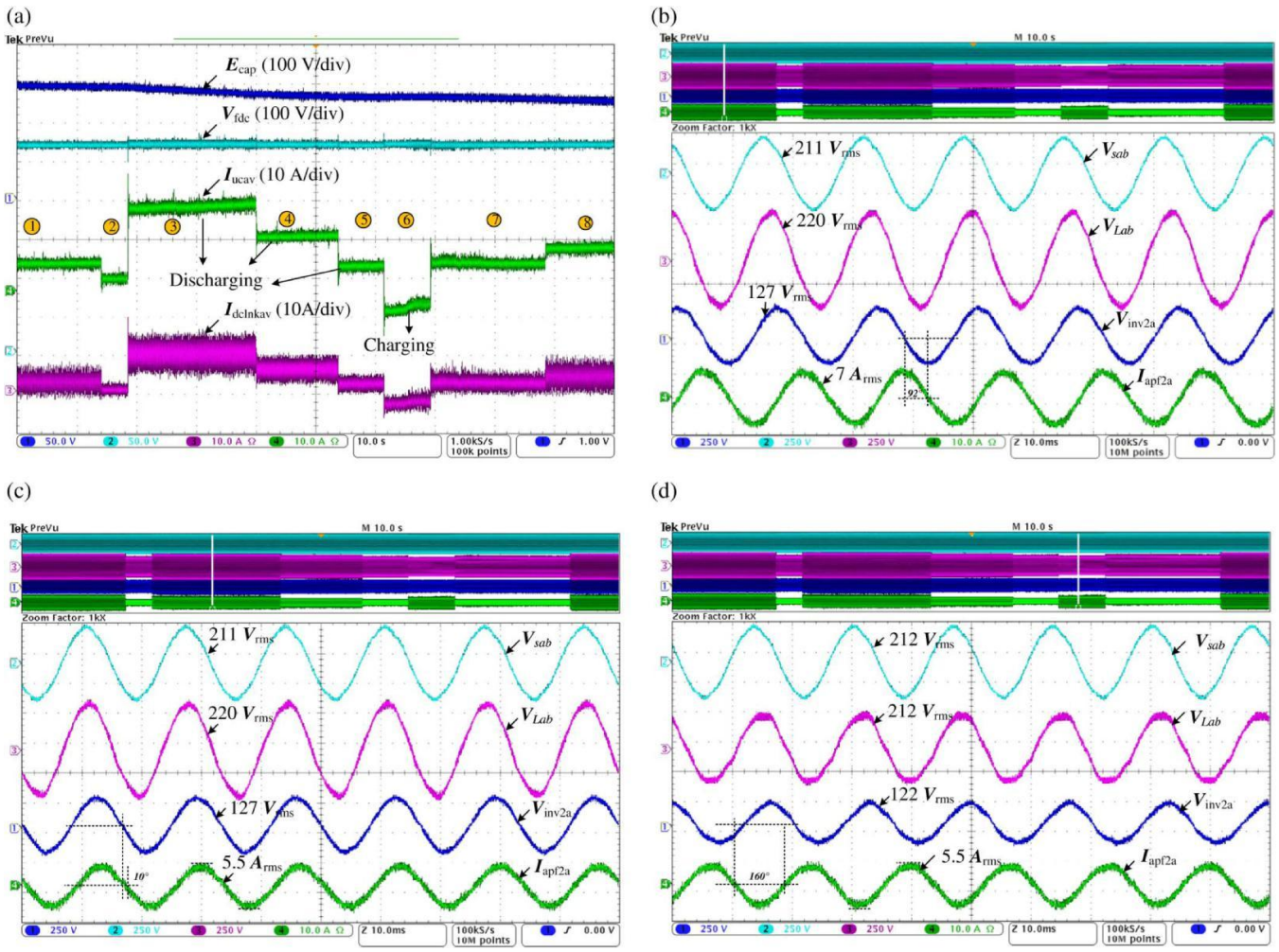


Fig. 11. (a) Bidirectional dc–dc converter waveforms showing UCAP-PC system performance V_{fdc} (CH1), E_{cap} (CH2), $I_{dclnkav}$ (CH3), and I_{ucav} (CH4).
(b) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3), and I_{apf2a} (CH4) for zone 1 (reactive power support $i_{dref} = -10.0A$). (c) Inverter experimental waveforms V_{sab} (CH1), V_{Lab} (CH2), V_{sa} (CH3), and I_{apf2a} (CH4) for zone 3 (active power support $i_{qref} = -8.0$ **A**). (d) Inverter experimental waveforms V_{ab} (CH1), V_{inv1a} (CH2), V_{sa} (CH3), and I_{apf2a} (CH4) for zone 6 (UCAP charging $i_{qref} = 7.0$ **A**).

7 in Fig. 10(a) that E_{cap} is almost constant while I_{ucav} and $I_{dclnkav}$ are almost zero, which proves that the active power discharged from the UCAP while providing reactive power support to the grid is minimal. In Fig. 11(c), the zoomed in view of zone 3 where the inverter is only providing active

power support to the grid by commanding $i_{qref} = -8.0$ A

and this can be concluded from the fact that I_{apf2a} and

V_{sa} are almost in phase with little phase difference around of 10°. The results are similar for zones 4 and 5, where the commanded active power is comparatively less than that in zone 3. It is important to notice zones 3–5 of Fig. 11(a) from which it can be observed that UCAP is discharging power rapidly in these zones therefore, E_{cap} is decreasing rapidly while V_{fdc} remains constant at 260 V and I_{ucav} is increasing rapidly, while $I_{dclnkav}$ remains almost constant. The bidirectional capability of the dc–dc converter and the inverter is necessary for absorbing excess power from DERs in renewable intermittency smoothing applications. To achieve this objective, i_{qref} is set to 7 A, and it can be observed from Fig. 11(d), which is the zoomed in view of zone 6 that phase difference between I_{apf2a} and V_{sa} is around 170°, which shows that the inverter is absorbing power from the grid. The bidirectional dc–dc converter operates in Buck mode to absorb power from the grid, which can be observed from zone 6 of Fig. 11(a), where both I_{ucav} and $I_{dclnkav}$ are negative, while V_{fdc} is at 260 V and E_{cap} is increasing slowly due to the UCAP being charged from the power which is absorbed from the grid.

In Fig. 12(a) and (b), the UCAP-PC system performance when the system experiences unbalanced voltage sag are presented. It can be observed from Fig. 12(a) that a 20% voltage sag is generated in phases *a* and *b*, the system voltages V_{sa} and V_{sb} experience a voltage sag. However, the inverter current I_{apf2a} remains constant at 7.5 A_{rms} while providing active power support to the grid even after the system experiences unbalanced voltage sag. This clearly indicates that the PLL tracks the fundamental component even during unbalanced scenarios, which allows the UCAP-APF system to provide active and reactive power support to the grid under unbalanced conditions. From the bidirectional dc–dc converter waveforms shown in Fig. 12(b), it can be observed that during the unbalanced voltage sag, which lasts for *1 s*, the dc-link voltage

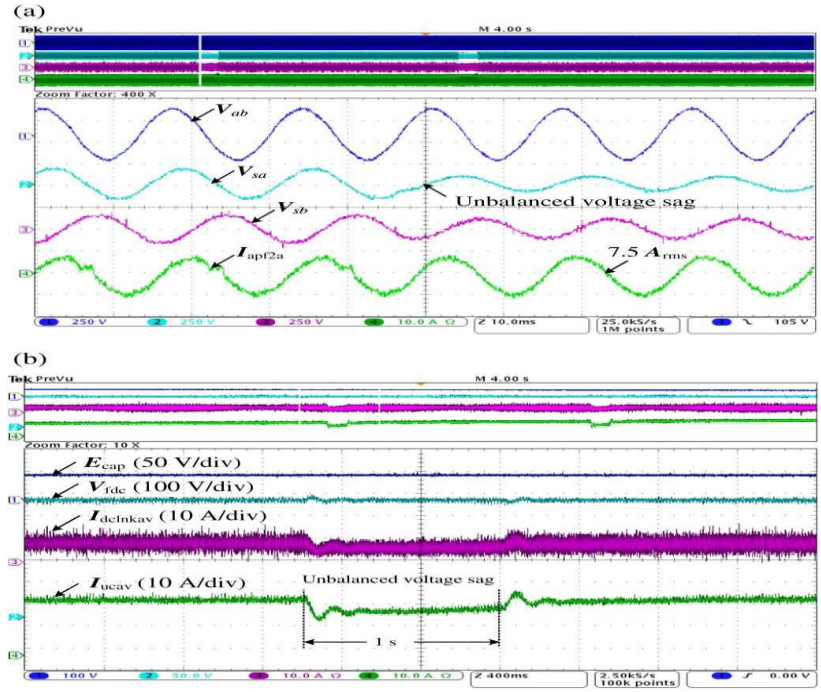


Fig. 12. (a) Series and shunt inverter experimental waveforms V_{ab} (CH1), V_{sa} (CH2), V_{sb} (CH3), and I_{apf2a} (CH4) for when PC provides active power support $i_{qref} = -12.0$ **A** during an unbalanced sag in phases *a* and *b*.

(b) Bidirectional dc–dc converter waveforms showing transient response in active power support mode during an unbalanced sag in phases *a* and

V_{fdc} has slight fluctuations and settles down to steady state value of 260 V very fast.

VI. CONCLUSION

In this paper, the concept of integrating UCAP-based rechargeable energy storage to a power conditioner system to improve the power quality of the distribution grid is presented. With this integration, the DVR portion of the power conditioner will be able to independently compensate voltage sags and swells and the APF portion of the power conditioner will be able to provide active/reactive power support and renewable intermittency smoothing to the distribution grid. UCAP integration through a bidirectional dc–dc converter at the dc-link of the power conditioner is proposed. The control strategy of the series inverter (DVR) is based on in-phase compensation and the control strategy of the shunt inverter (APF) is based on $i_d - i_q$ method. Designs of major components in the power stage of the bidirectional dc–dc converter are discussed. Average current mode control is used to regulate the output voltage of the dc–dc converter due to its inherently stable characteristic. A higher level integrated controller that takes decisions based on the system parameters provides inputs to the inverters and dc–dc converter controllers to carry out their control actions. The simulation of the integrated UCAP-PC system which consists of the UCAP, bidirectional dc–dc converter, and the series and shunt inverters is carried out using PSCAD. The simulation of the UCAP-PC system is carried out using PSCAD. Hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag compensation and active/reactive power support and renewable intermittency smoothing to the distribution grid is tested. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP-based energy storages can be deployed in the future in a microgrid or a low-voltage distribution grid to respond to dynamic changes in the voltage profiles and power profiles on the distribution grid.

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