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A Novel Implementation of Dynamic Voltage Restorer-Ultracapacitor Design For IMPROVING Power Quality Of The Distribution Grid

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Abstract: Cost of various energy storage technologies is decreasing rapidly and the integration of these technologies into the power grid is becoming a reality with the advent of smart grid. Dynamic voltage restorer (DVR) is one product that can provide improved voltage sag and swell compensation with energy storage integration. Ultra capacitors (UCAP) have low-energy density and high-power density ideal characteristics for compensation of voltage sags and voltage swells, which are both events that require high power for short spans of time. The novel contribution of this paper lies in the integration of rechargeable UCAP-based energy storage into the DVR topology. With this integration, the UCAP-DVR system will have active power capability and will be able to independently compensate temporary voltage sags and swells without relying on the grid to compensate for faults on the grid like in the past. UCAP is integrated into dc-link of the DVR through a bidirectional dc–dc converter, which helps in providing a stiff dc-link voltage, and the integrated UCAP-DVR system helps in compensating temporary voltage sags and voltage swells, which last from 3 s to 1 min. Complexities involved in the design and control of both the dc–ac inverter and the dc–dc converter are discussed.

INTRODUCTION

The electric power system is considered to be composed of three functional blocks - generation, transmission and distribution. For a reliable power system, the generation unit must produce adequate power to meet customer's demand, transmission systems must transport bulk power over long distances without overloading or jeopardizing system stability and distribution systems must deliver electric power to each customer's premises from bulk power systems. Distribution system locates the end of power system and is connected to the customer directly, so the power quality mainly depends on distribution system. The reason behind this is that the electrical distribution network failures account for about 90% of the average customer interruptions. In the earlier days, the major focus for power system reliability was on generation and transmission only as these more capital cost is involved in these. In addition their insufficiency can cause widespread catastrophic consequences for both society and its environment. But now a day's distribution systems have begun to receive more attention for reliability assessment.

Initially for the improvement of power quality or reliability of the system FACTS devices like static synchronous compensator (STATCOM), static synchronous series compensator (SSSC), interline power flow controller (IPFC), and unified power flow controller (UPFC) etc are introduced. These FACTS devices are designed for the transmission system. But now a day's more attention is on the distribution system for the improvement of power quality, these devices are modified and known as custom power devices. The main custom power devices which are used in distribution system for power quality improvement are distribution static synchronous compensator (DSTATCOM), dynamic voltage Restorer (DVR), active filter (AF), unified power quality conditioner (UPQC) etc.

In this thesis work from the above custom power devices, DVR is used with PI controller for the power quality improvement in the distribution system. Here two different loads are considered, one is linear load and the other is induction motor. Different fault conditions are considered with these loads to analyze the operation of DVR to improve the power quality in distribution system.

II. THREE-PHASE SERIES INVERTER

A. Power Stage

The one-line diagram of the system is shown in Fig. 1. The power stage is a three-phase voltage source inverter, which is connected in series to the grid and is responsible for compensating the voltage sags and swells; the model of the series DVR and its controller is shown in Fig. 2. The inverter system consists of an insulated gate bipolar transistor (IGBT) module, its gate-driver, *LC* filter, and an isolation transformer. The dc-link voltage *V*dc is regulated at 260 V for optimum performance of the converter and the line–line voltage *Vab* is 208 V; based on these, the modulation index *m* of the inverter is given by

$$m = \frac{2\sqrt{2}}{\sqrt{3}V_{\mathrm{dc}}*n} V_{ab(\mathrm{rms})}. \qquad (1)$$

Where *n* is the turns ratio of the isolation transformer. Substituting *n* as 2.5 in (1), the required modulation index is calculated as 0.52. Therefore, the output of the dc–dc converter should be regulated at 260 V for providing accurate voltage compensation. The objective of the integrated UCAPDVR system with active power capability is to compensate for *temporary voltage sag* (0.1–0.9 p.u.) and *voltage swell* (1.1–1.2 p.u.), which last from 3 s to 1 min [15].

B. Controller Implementation

There are various methods to control the series inverter to provide dynamic voltage restoration and most of them rely on injecting a voltage in quadrature with advanced phase, so that reactive power is utilized in voltage restoration [3]. Phase advanced voltage restoration techniques are complex in implementation, but the primary reason for using these techniques is to minimize the active power support and thereby the amount of energy storage requirement at the dc-link in order to minimize the cost of energy storage. However, the cost of energy storage has been declining and with the availability of *active power support* at the dc-link, complicated phase-advanced techniques can be avoided and voltages can be injected *in-phase* with the system voltage during voltage sag or a swell event. The control method requires the use of a PLL to find the rotating angle. As discussed previously, the goal of this project is to use the *active power capability* of the UCAP-DVR system and compensate temporary voltage sags and swells.

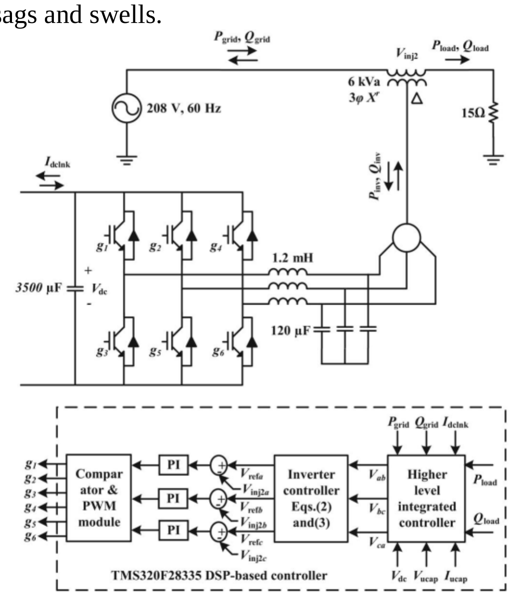

Fig. 2. Model of three-phase series inverter (DVR) and its controller with integrated higher order controller.

The inverter controller implementation is based on injecting voltages *in-phase* with the supply-side line–neutral voltages. This requires PLL for estimating θ, which has been implemented using the *fictitious power method* described in [18].

Based on the estimated θ and the line–line source voltages, *Vab*, *Vbc*, and *Vca* (which are available for this delta-sourced system) are transformed into the *d*–*q* domain and the line– neutral components of the source voltage *Vsa*, *Vsb*, and *Vsc*, which are not available, can then be estimated using

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta - \frac{\pi}{6}\right) & \sin\left(\theta - \frac{\pi}{6}\right) \\ -\sin\left(\theta - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} \frac{V_d}{\sqrt{3}} \\ \frac{V_q}{\sqrt{3}} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} V_{\text{ref}a} \\ V_{\text{ref}b} \\ V_{\text{ref}c} \end{bmatrix} = m* \begin{bmatrix} \left(\sin\theta - \frac{V_{sa}}{169.7}\right) \\ \left(\sin\left(\theta - \frac{2\pi}{3}\right) - \frac{V_{sb}}{169.7}\right) \\ \left(\sin\left(\theta + \frac{2\pi}{3}\right) - \frac{V_{sc}}{169.7}\right) \end{bmatrix} \quad (3)$$

$$P_{\text{inv}} = 3V_{\text{inj}2a(\text{rms})} I_{La(\text{rms})} \cos\varphi$$
$$Q_{\text{inv}} = 3V_{\text{inj}2a(\text{rms})} I_{La(\text{rms})} \sin\varphi. \quad (4)$$

III. UCAP AND BIDIRECTIONAL DC–DC CONVERTER

A. UCAP Setup

The choice of the number of UCAPs necessary for providing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage, and distribution grid voltages. In this paper, the experimental setup consists of three 48 V, 165F UCAPs (BMOD0165P048) manufactured by Maxwell Technologies, which are connected in series. Therefore, the terminal voltage of the UCAP bank is 144 V and the dc-link voltage is programmed to 260 V. This would give the dc–dc converter a practical operating duty ratio of 0.44–0.72 in the *boost mode* while the UCAP is discharging and 0.27– 0.55 in the *buck mode* while the UCAP is charging from the grid through the dc-link and the dc–dc converter. It is practical and cost-effective to use three modules in the UCAP bank.

Assuming that the UCAP bank can be discharged to 50% of its initial voltage (Vuc,ini) to final voltage (Vuc,fin) from 144 to 72 V, which translates to depth of discharge of 75%, the energy in the UCAP bank available for discharge is given by

$$E_{\text{UCAP}} = \frac{1}{2} * C * \frac{\left(V_{\text{uc,ini}}{}^2 - V_{\text{uc,fin}}{}^2\right)}{60} W - \text{min}$$
$$E_{\text{UCAP}} = 1/2*165/3*\left(144^2 - 72^2\right)/60$$
$$= 7128 \text{ W} - \text{min}. \quad (5)$$

B. Bidirectional DC–DC Converter and Controller

A UCAP cannot be directly connected to the dc-link of the inverter like a battery, as the voltage profile of the UCAP varies as it discharges energy. Therefore, there is a need to integrate the UCAP system through a bidirectional dc–dc converter, which maintains a stiff dc-link voltage, as the UCAP voltage decreases while *discharging* and increases while *charging*. The model of the bidirectional dc–dc converter and its controller are shown in Fig. 3, where the input consists of three UCAPs connected in series and the output consists of a nominal load of 213.5 Ω to prevent operation at no-load, and the output is connected to the dc-link of the inverter. The amount of active power support required by the grid during a voltage sag event is dependent on the depth and duration of the voltage sag, and the dc–dc converter should be able to withstand this power during the *discharge* mode. The dc–dc converter should also be able to operate in bidirectional mode to be able to *charge* or absorb additional power from the grid during voltage swell event. In this paper, the bidirectional dc–dc converter acts as a boost converter while *discharging* power from the UCAP and acts as a buck converter while *charging* the UCAP from the grid.

A bidirectional dc–dc converter is required as an interface between the UCAP and the dc-link since the UCAP voltage varies with the amount of energy discharged while the dc-link voltage has to be stiff. Therefore, the bidirectional dc–dc converter is designed to operate in boost mode when the UCAP bank voltage is between 72 and 144 V and the output voltage is regulated at 260 V. When the UCAP bank voltage is below 72 V, the bidirectional dc–dc converter is operated in buck mode and draws energy from the grid to charge the UCAPs and the output voltage is again regulated at 260 V.

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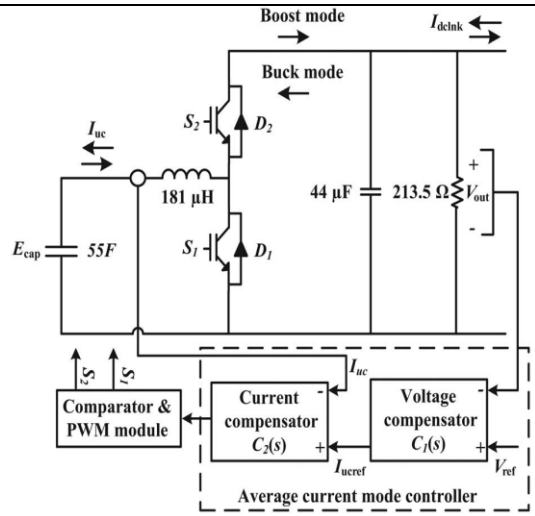


Fig. 3. Model of the bidirectional dc–dc converter and its controller.

Average current mode control, which is widely explored in literature [19], is used to regulate the output voltage of the bidirectional dc–dc converter in both *buck* and *boost* modes while *charging* and *discharging* the UCAP bank. This method tends to be more stable when compared to other methods such as voltage mode control and peak current mode control. Average current mode controller is shown in Fig. 3, where the dc-link and actual output voltage *V*out is compared with the reference voltage *V*ref and the error is passed through the voltage compensator *C*1(*s*), which generates the average reference current *I*ucref .When the inverter is *discharging* power into the grid during voltage sag event, the dc-link voltage *V*out tends to go below the reference *V*ref and the error is positive; *I*ucref is positive and the dc–dc converter operates in *boost* mode. When the inverter is absorbing power from the grid during voltage swell event or *charging* the UCAP, *V*out tends to increase above the reference *V*ref and the error is negative; *I*ucref is negative and the dc–dc converter operates in *buck* mode. Therefore, the sign of the error between *V*out and *V*ref determines the sign of *I*ucref and thereby the direction of operation of the bidirectional dc–dc converter. The reference current *I*ucref is then compared to the actual UCAP current (which is also the inductor current) *I*uc and the error is then passed through the current compensator *C*2(*s*). The compensator transfer functions, which provide a stable response, are given by

$$C_1(s) = 1.67 + \frac{23.81}{s} \quad (6)$$

$$C_2(s) = 3.15 + \frac{1000}{s}. \quad (7)$$

IV SIMULINK MODEL OF THE TEST SYSTEM

The simulation of the proposed UCAP-integrated DVR system is carried out in PSCAD for a 208 V, 60-Hz system where 208 V is 1 p.u. The system response for a three-phase voltage sag, which lasts for 0.1 s and has a depth of 0.84 p.u., is shown in Fig. 4(a)–(e). It can be observed from Fig. 4(a) that during voltage sag, the source voltage *Vs*rms is reduced to 0.16 p.u. while the load voltage *VL*rms is maintained constant at around 0.9 p.u. due to voltages injected *in-phase* by the series inverter.

This can also be observed from the plots of the line–line source voltages [*Vsab*, *Vsbc*, *Vsca*; Fig. 4(b)], the line–line load voltages [*VLab*, *VLbc*, *VLca*; Fig. 4(c)], and the line–neutral injected voltages of the series inverter [*V*inj2*a*, *V*inj2*b*, *V*inj2*c*; Fig. 4(d)]. Finally, it can be observed from Fig. 4(e) that *V*inj2*a* lags *Vsab* by 30◦, which indicates that it is *in-phase* with the line–neutral source voltage *Vsa*. In Fig. 5(a), plots of the bidirectional dc–dc converter are presented and it can be observed that the dc-link voltage *Vf*dc is regulated at 260 V, the average dc-link current *I*dclnkav and the average UCAP current *I*ucav increase to provide the active power required by the load during the sag. Although the UCAP is discharging, the change in the UCAP voltage *E*cap is not visible in this case due to the short duration of the simulation, which is due to limitations in PSCAD software. It can also be observed from the various active power plots shown in Fig. 5(b) where the power supplied to the load *P*load remains constant even during the voltage sag when the grid power *P*grid is decreasing. The active power deficit of the grid is met by the inverter power *P*inv, which is almost equal to the input power to the inverter *P*dc_*n* available from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and the load during the voltage sag event is being met by the integrated

UCAP-DVR system through the bidirectional dc–dc converter and the inverter. Similar analysis can also be extended for voltage sags, which occur in one of the phases (*a*, *b*, or *c*) or in two of the phases (*ab*, *bc*, or *ca*). However, the active power requirement is greatest for the case where all the three phases ABC experience voltage sag.

The system response for a three-phase voltage swell, which lasts for 0.1 s and has a magnitude of 1.2 p.u., is shown in Fig. 6(a)–(e). It can be observed that during voltage swell, the source voltage *Vs*rms increases to 1.2 p.u., whereas the load voltage *VL*rms is maintained constant at around 1 p.u. due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line–line source voltages [*Vsab, Vsbc, Vsca*; Fig. 6(a)], the line–line load voltages [*VLab, VLbc, VLca*; Fig. 6(b)], and the line–neutral injected voltages of the series inverter [*V*inj2*a, V*inj2*b, V*inj2*c*; Fig. 6(c)].

Finally, it can be observed that *V*inj2*a* lags *Vsab* by 150◦, which indicates that it is 180◦ out of phase with the line–neutral source voltage *Vsa* as required by the in-phase control algorithm.

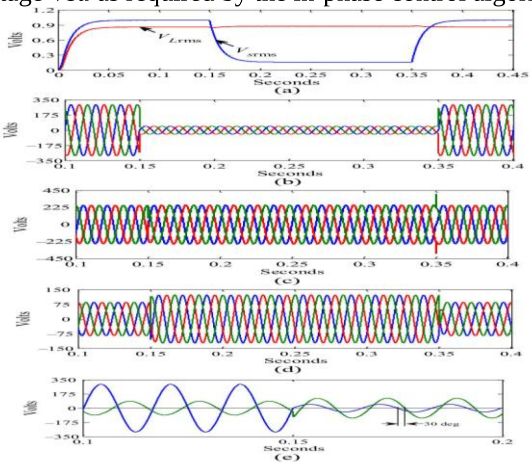


Fig. 4. (a) Source and load RMS voltages *Vs*rms and *VL*rms during sag.(b) Source voltages *Vsab* (blue), *Vsbc* (red), and *Vsca* (green) during sag.(c) Load voltages *VLab* (blue), *VLbc* (red), and *VLca* (green) during sag.(d) Injected voltages *V*inj2*a* (blue), *V*inj2*b* (red), and *V*inj2*c* (green) during sag.(e) *V*inj2*a* (green) and *Vsab* (blue) waveforms during sag.

In Fig. 7(a), plots of the bidirectional dc–dc converter are presented and it can be observed that the dc-link voltage *Vf*dc is regulated at 260 V, the average dc-link current *I*dclnkav and the average UCAP current *I*ucav change direction to absorb the additional active power from the grid into the UCAP during the voltage swell event. The overshoot in *I*ucav and *I*dclnkav during startup at 0.1 s and during mode changes at 0.15 and 0.35 s is due to the mismatch between the breaker action and the compensator action in PSCAD, which is a modeling problem present in the simulation results.

Again, due to PSCAD limitations, which restrict the duration of the simulation, the increase in *E*cap due to charging of the UCAP during the voltage swell is not visible. This can also be observed from various active power plots where the power supplied to the load *P*load remains constant even during the voltage swell when the grid power *P*grid is increasing.

It can be observed from the inverter power *P*inv and inverter input power *P*dc_in plots that the additional active power from the grid is absorbed by the inverter and transmitted to the UCAP. Therefore, it can be concluded from the plots that the additional active power from the grid during the voltage swell event is being absorbed by the UCAP-DVR system through the bidirectional dc–dc converter and the inverter.

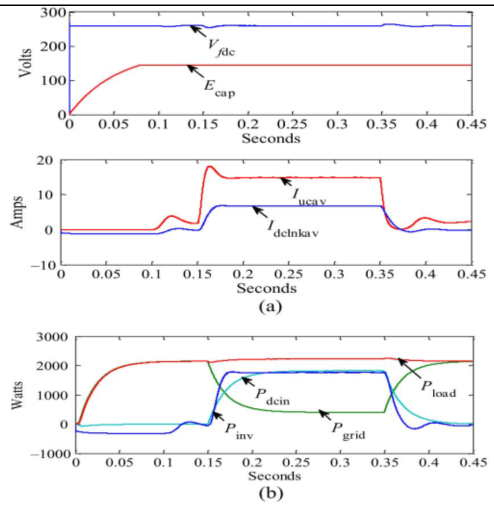


Fig. 5. (a) Currents and voltages of dc–dc converter. (b) Active power of grid, Load, and inverter during voltage sag.

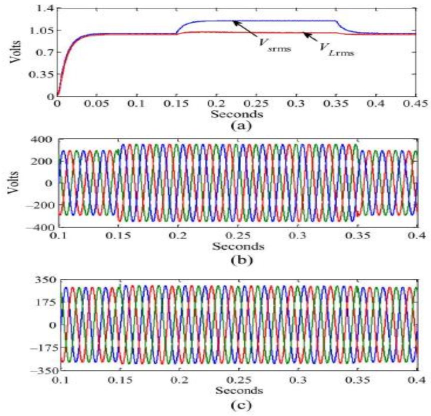
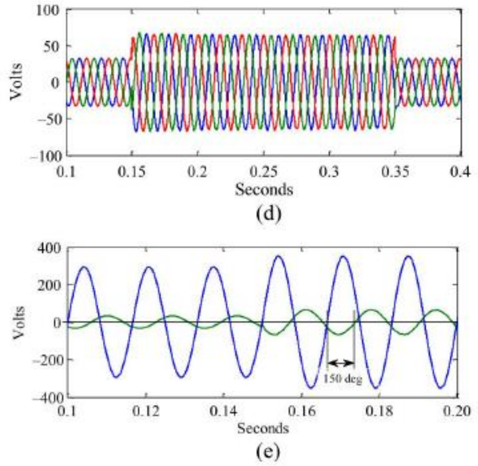


Fig. 6. (a) Source and load rms voltages *Vsrms* and *VLrms* during swell. (b) Source voltages *Vsab* (blue), *Vsbc* (red), and *Vsca* (green) during swell. (c) Load voltages *VLab* (blue), *VLbc* (red), and *VLca* (green) during swell.



(d) Injected voltages *V*inj2*a* (blue), *V*inj2*b* (red), *V*inj2*c* (green) during swell. (e) *V*inj2*a* (green) and *Vsab* (blue) waveforms during swell.

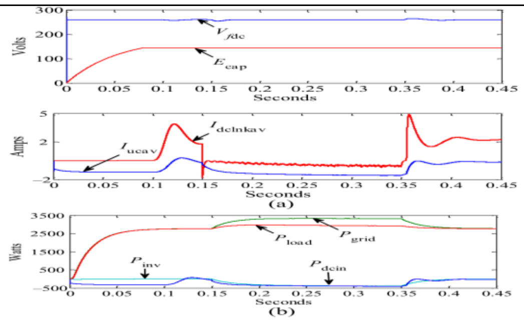


Fig. 7. (a) Currents and voltages of dc–dc converter during swell. (b) Active and reactive power of grid, load, and inverter during a voltage swell.

CONCLUSION

In this work, a fast and cost effective Dynamic Voltage Restorer (DVR) is proposed for mitigating the problem of voltage sag or dip and other fault conditions in industrial distribution systems, specially consisting of the induction motor load. A controller which is based on feed foreword technique is used which utilizes the error signal which is the difference between the reference voltage and actual measured load voltage to trigger the switches of an inverter using a Pulse Width Modulation (PWM) scheme. Here, investigations were carried out for various cases of load at 11kv feeder. It is clear from the results that the power quality of the system with induction motor as load is increased in the sense that the THD and the amount of unbalance in load voltage are decreased with the application of DVR. The effectiveness of DVR using PI controller is established both for linear static load and induction motor load.

In this paper, the concept of integrating UCAP-based rechargeable energy storage to the DVR system to improve its voltage restoration capabilities is explored. With this integration, the DVR will be able to independently compensate voltage sags and swells without relying on the grid to compensate for faults on the grid. The UCAP integration through a bidirectional dc–dc converter at the dc-link of the DVR is proposed. The power stage and control strategy of the series inverter, which acts as the DVR, are discussed. The control strategy is simple and is based on injecting voltages in-phase with the system voltage and is easier to implement when the DVR system has the ability to provide active power. A higher level integrated controller, which takes decisions based on the system parameters, provides inputs to the inverter and dc–dc converter controllers to carry out their control actions. Designs of major components in the power stage of the bidirectional dc–dc converter are discussed.

Average current mode control is used to regulate the output voltage of the dc–dc converter due to its inherently stable characteristic. The simulation of the UCAP-DVR system, which consists of the UCAP, dc–dc converter, and the grid-tied inverter, is carried out using PSCAD. Hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag and swell compensation in all three phases to the distribution grid dynamically is tested. Results for transient response during voltage sags/swells in two phases will be included in the full-version of this paper. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAPbased energy storages can be deployed in the future on the distribution grid to respond to dynamic changes in the voltage profiles of the grid and prevent sensitive loads from voltage disturbances.

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